FIG. 1

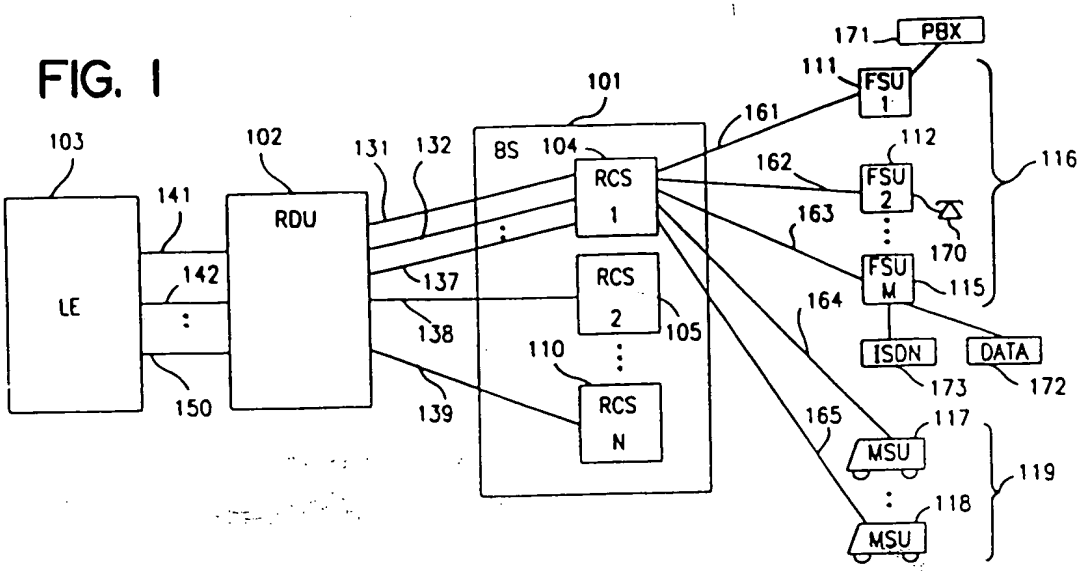


FIG. 2a

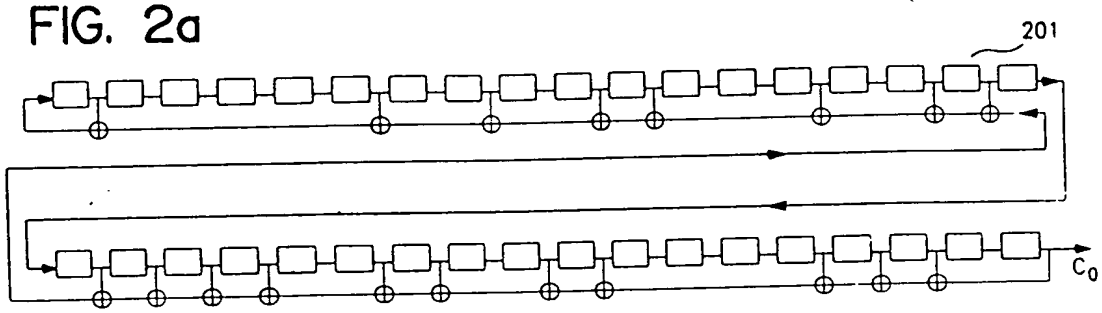


FIG. 2b

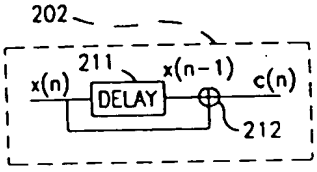


FIG. 2c

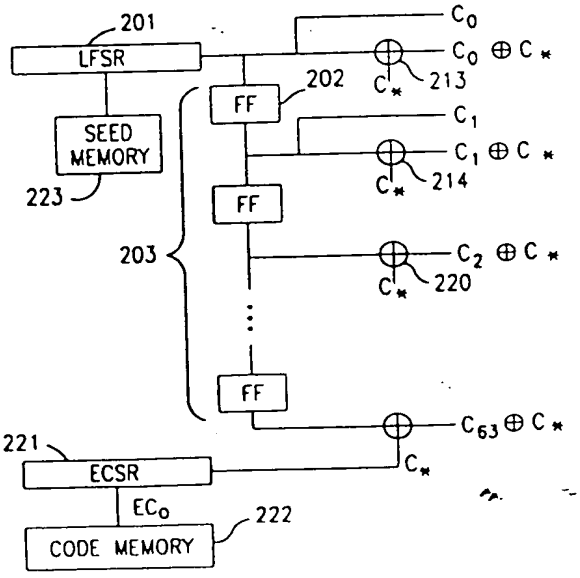
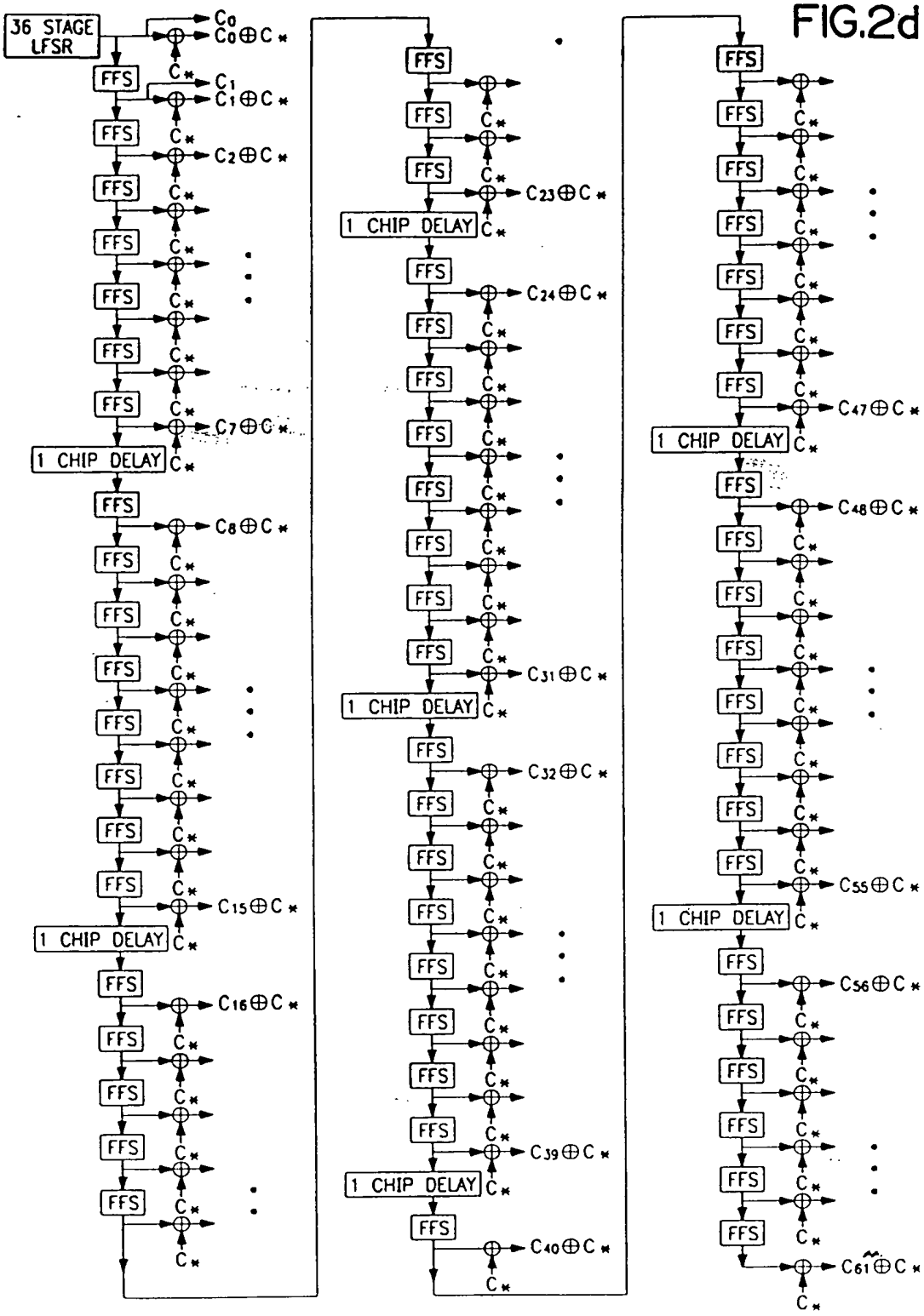


FIG.2d


36 STAGE LFSR
FFS
1 CHIP DELAY
C0
C0⊕C*
C1
C1⊕C*
C2⊕C*
C7⊕C*
C8⊕C*
C15⊕C*
C16⊕C*
C23⊕C*
C24⊕C*
C31⊕C*
C32⊕C*
C39⊕C*
C40⊕C*
C47⊕C*
C48⊕C*
C55⊕C*
C56⊕C*
C61⊕C*
C*

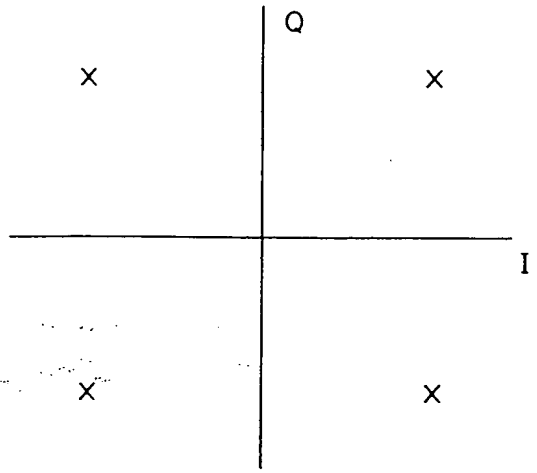


FIG. 3a

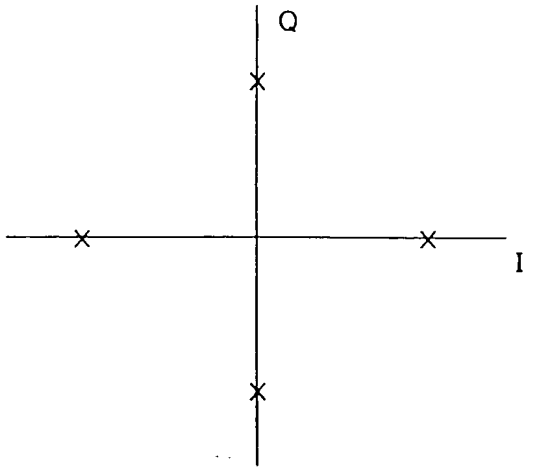


FIG. 3b

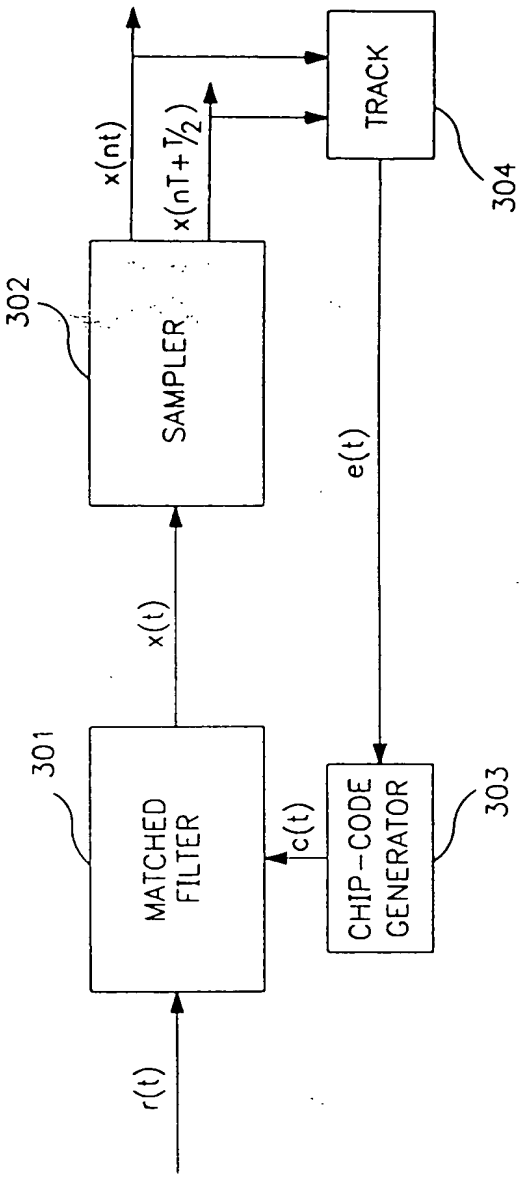

r(t)
MATCHED FILTER
301
x(t)
SAMPLER
302
x(nt)
x(nT+T/2)
TRACK
304
e(t)
c(t)
CHIP-CODE GENERATOR
303

FIG. 3c

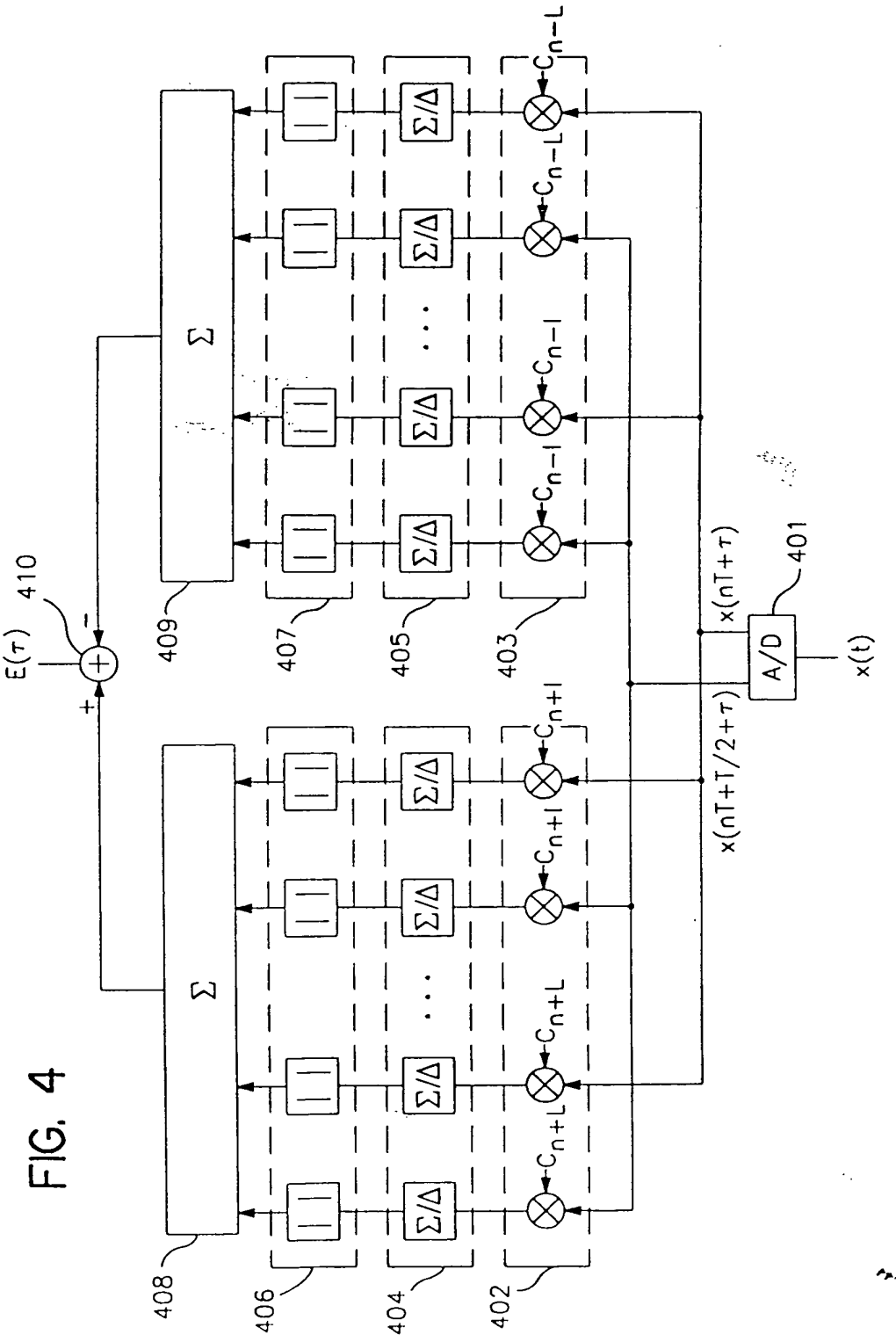

E(τ)
410
409
407
405
403
401
x(nT+τ)
x(nT+T/2+τ)
A/D
x(t)
408
406
404
402
Σ
Σ/Δ
C_{n-L}
C_{n-1}
C_{n+1}
C_{n+L}

FIG. 4

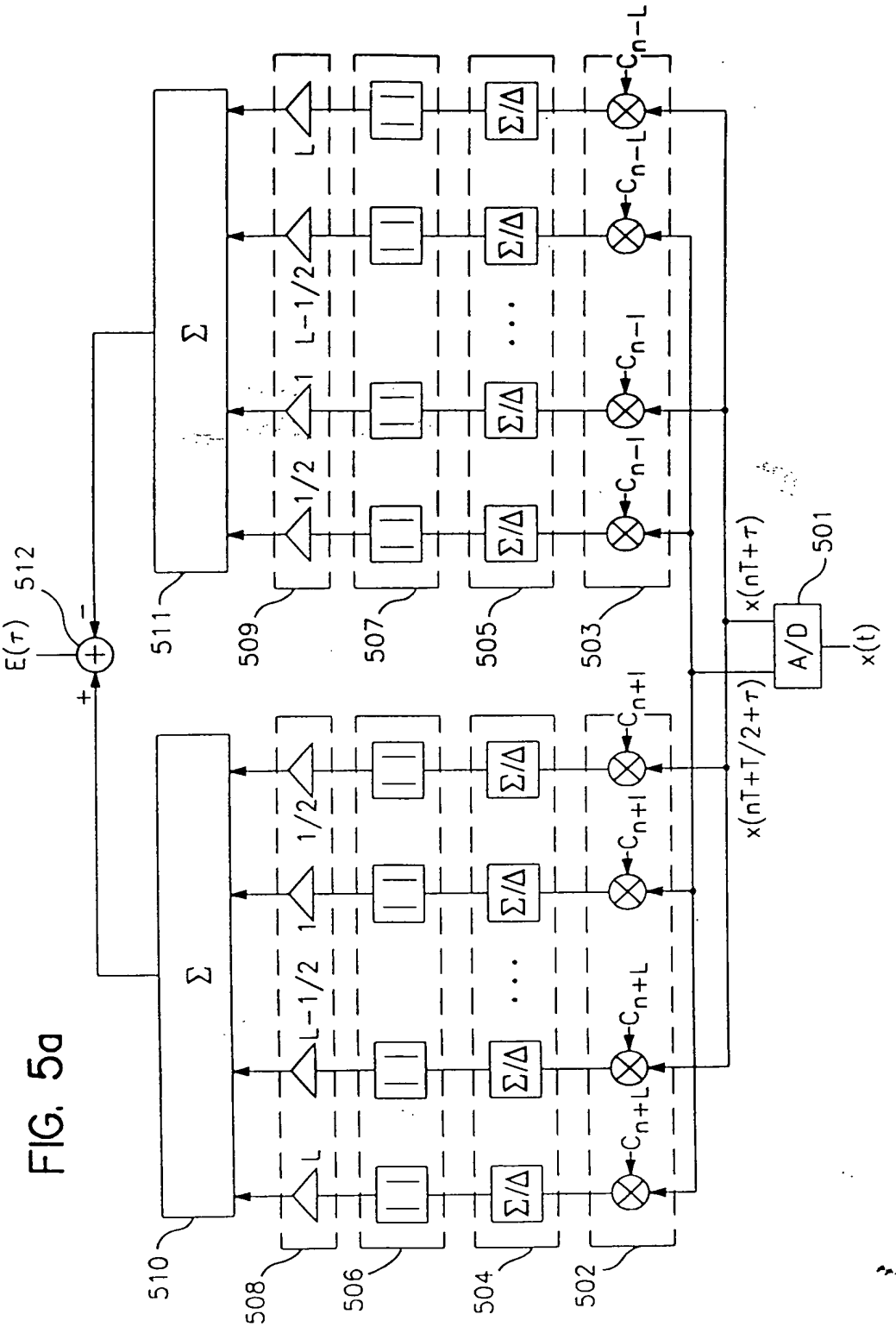
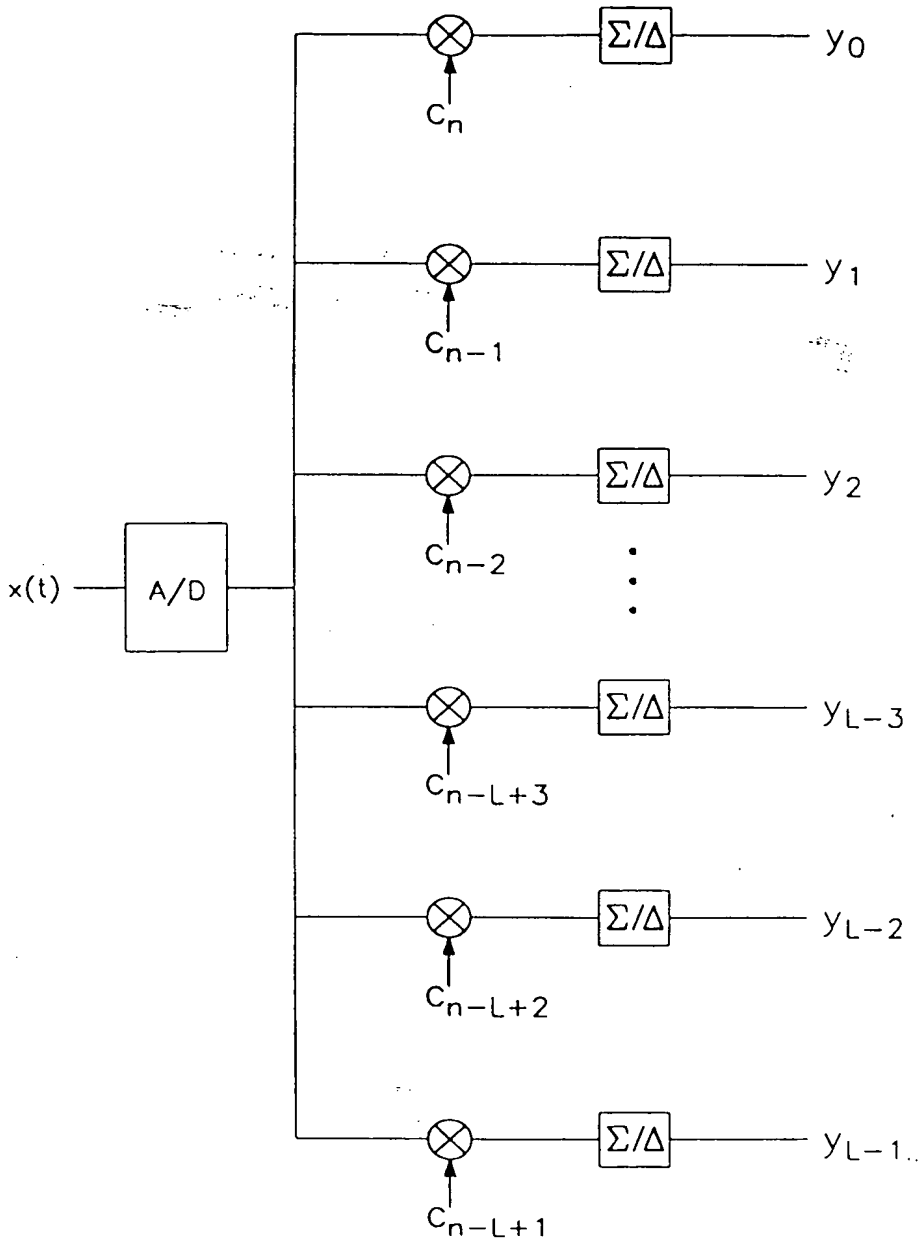

E(τ)
512
+
−
Σ
511
509
507
505
503
L
L-1/2
1
1/2
Σ/Δ
C_{n-L}
C_{n-L}
C_{n-1}
C_{n-1}
x(nT+τ)
501
A/D
x(t)
x(nT+T/2+τ)
C_{n+1}
C_{n+1}
C_{n+L}
C_{n+L}
510
508
506
504
502

FIG. 5a

FIG. 5b


x(t)
A/D
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
Σ/Δ
y_0
y_1
y_2
y_{L-3}
y_{L-2}
y_{L-1}
C_n
C_{n-1}
C_{n-2}
C_{n-L+3}
C_{n-L+2}
C_{n-L+1}

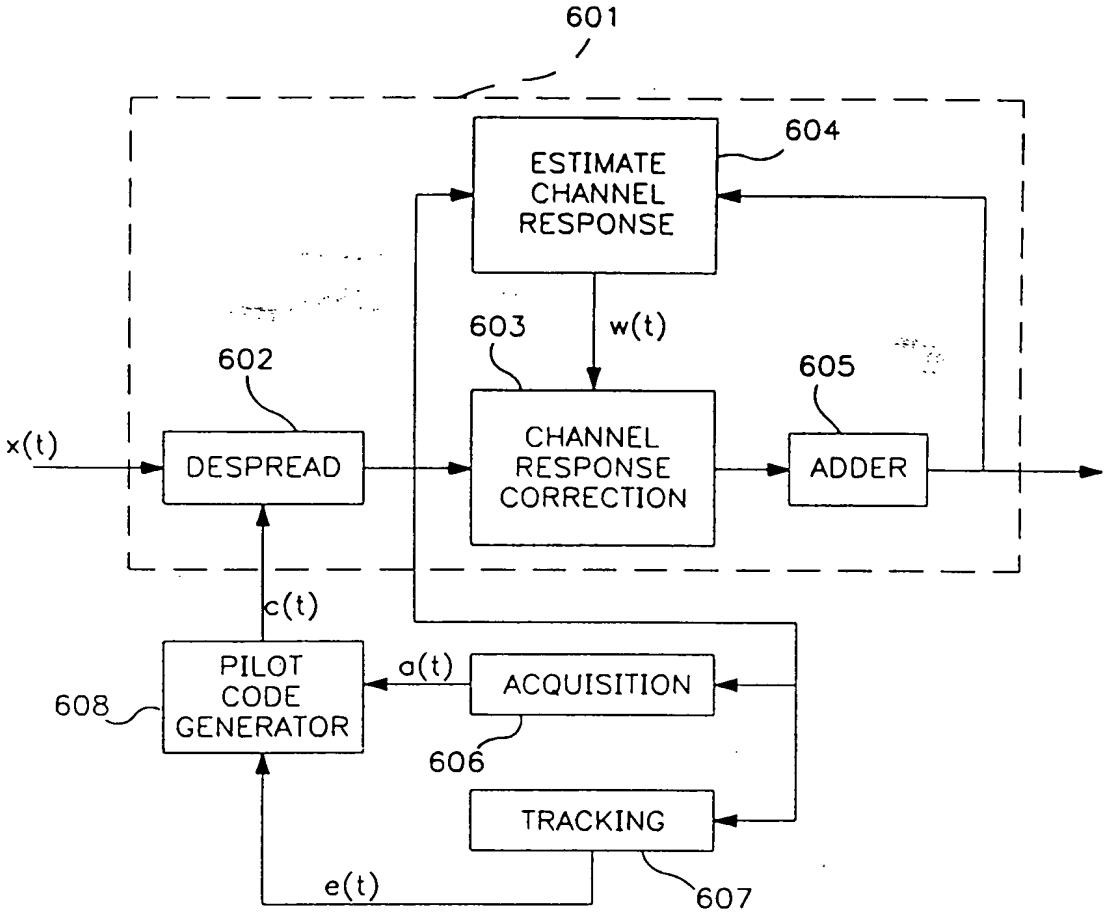

601
604
ESTIMATE CHANNEL RESPONSE
603
w(t)
602
605
x(t)
DESPREAD
CHANNEL RESPONSE CORRECTION
ADDER
c(t)
PILOT CODE GENERATOR
608
a(t)
ACQUISITION
606
TRACKING
e(t)
607

FIG. 6

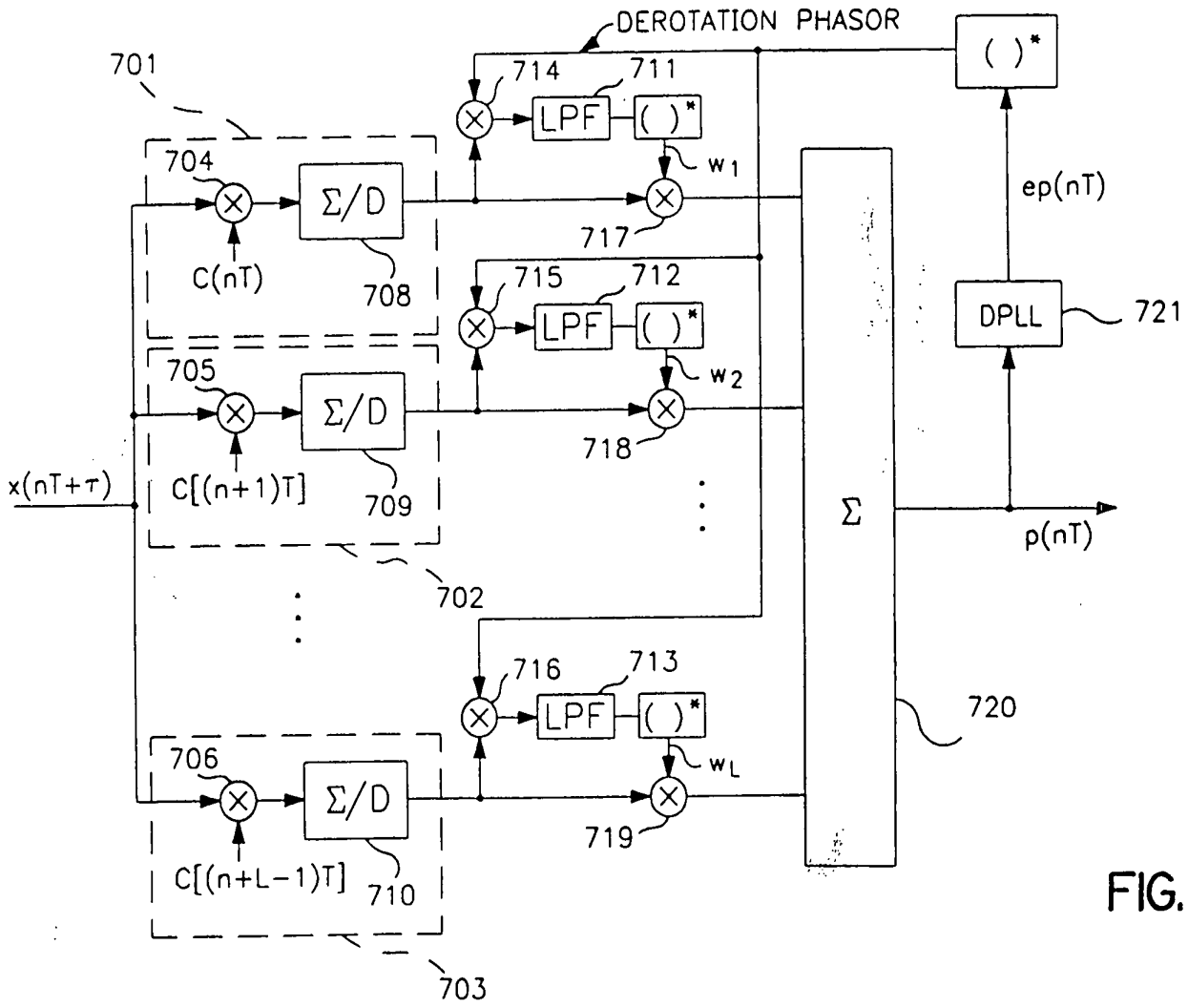

DEROTATION PHASOR
()*
701
714
711
LPF
()*
w1
704
Σ/D
C(nT)
708
717
ep(nT)
715
712
LPF
()*
w2
DPLL
721
705
Σ/D
718
x(nT+τ)
C[(n+1)T]
709
Σ
p(nT)
702
716
713
LPF
()*
720
wL
706
Σ/D
719
C[(n+L-1)T]
710
703

FIG. 7

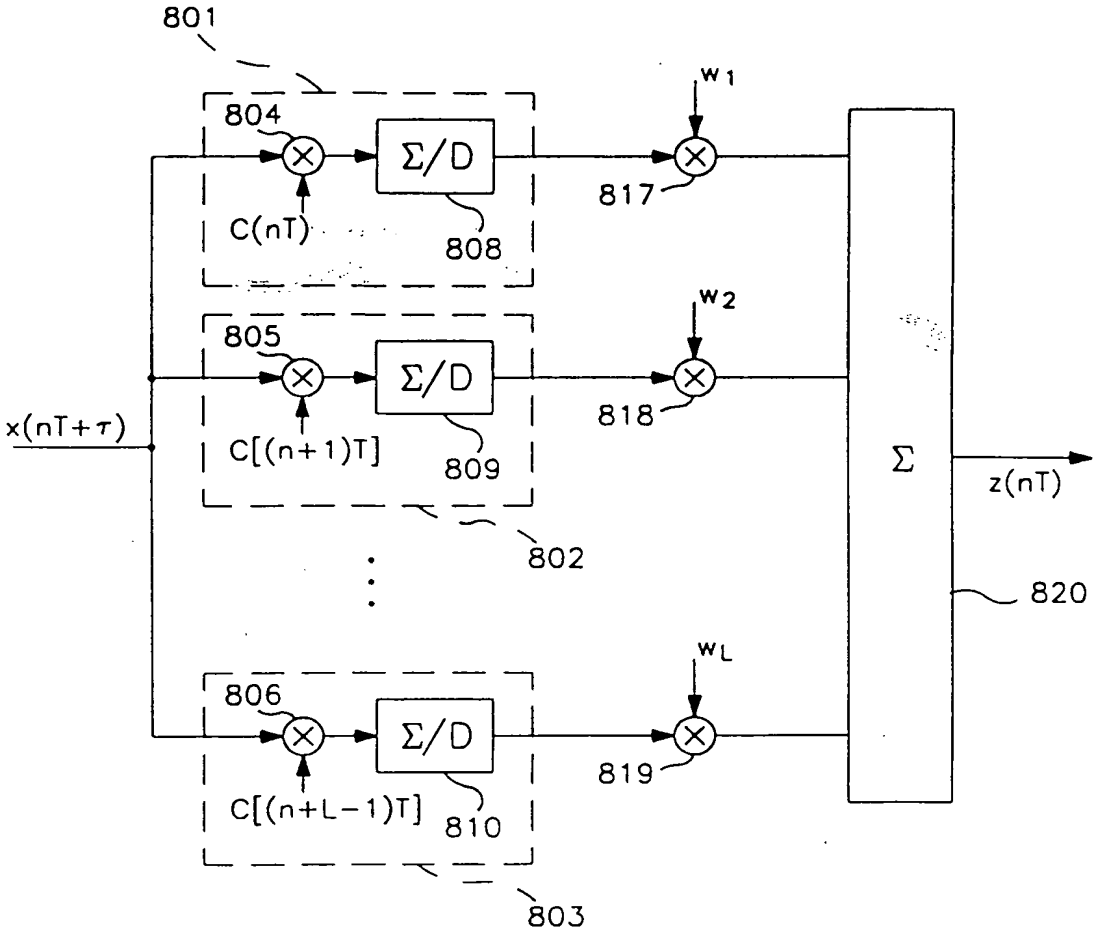

801
804
Σ/D
C(nT)
808
817
w_1
805
Σ/D
C[(n+1)T]
809
818
w_2
802
x(nT+τ)
Σ
z(nT)
820
806
Σ/D
C[(n+L−1)T]
810
819
w_L
803

FIG. 8a

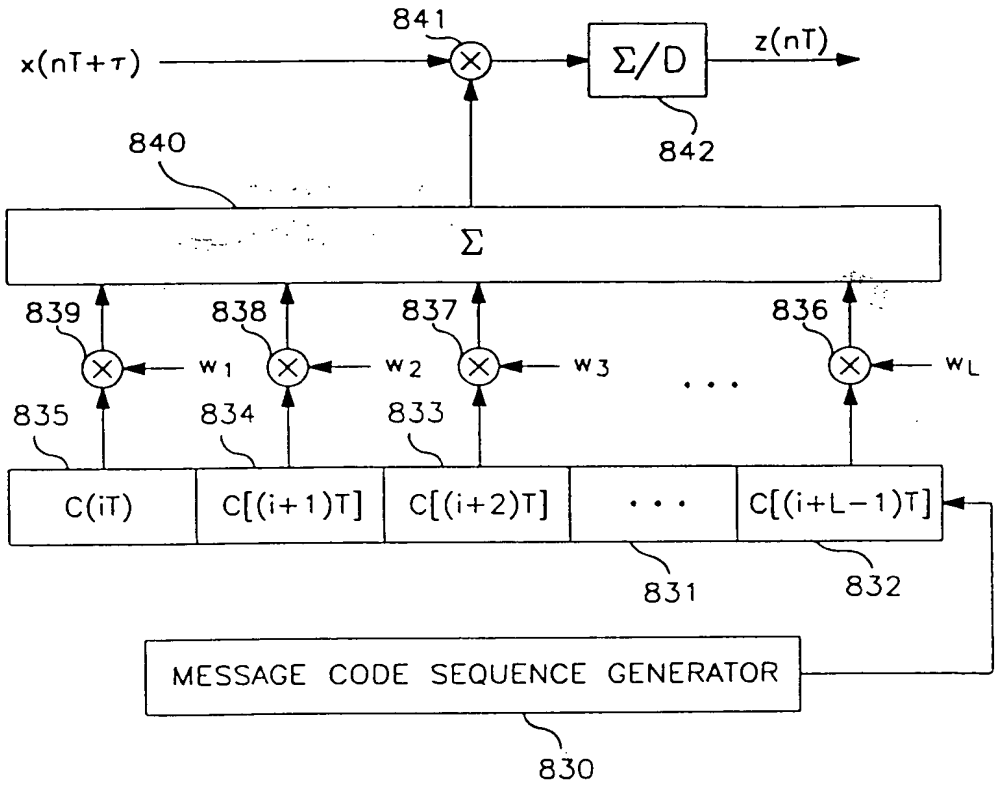

841
x(nT+τ)
Σ/D
z(nT)
842
840
Σ
839
838
837
836
w1
w2
w3
wL
835
834
833
C(iT)
C[(i+1)T]
C[(i+2)T]
C[(i+L−1)T]
831
832
MESSAGE CODE SEQUENCE GENERATOR
830

FIG. 8b

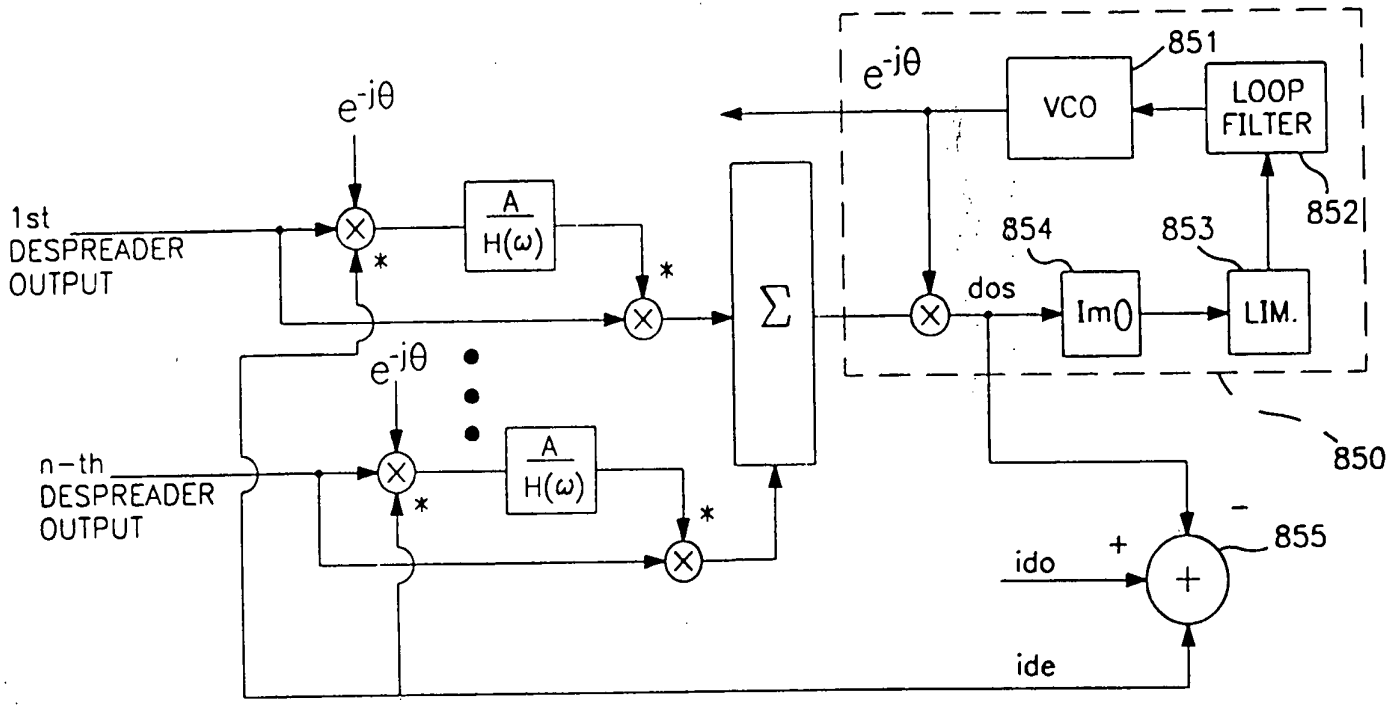

1st
DESPREADER
OUTPUT
n-th
DESPREADER
OUTPUT
e-jθ
e-jθ
e-jθ
A
H(ω)
A
H(ω)
*
*
*
*
Σ
e-jθ
VCO
LOOP
FILTER
851
852
853
854
dos
Im()
LIM.
850
855
ido
ide
+
+
−

FIG. 8c

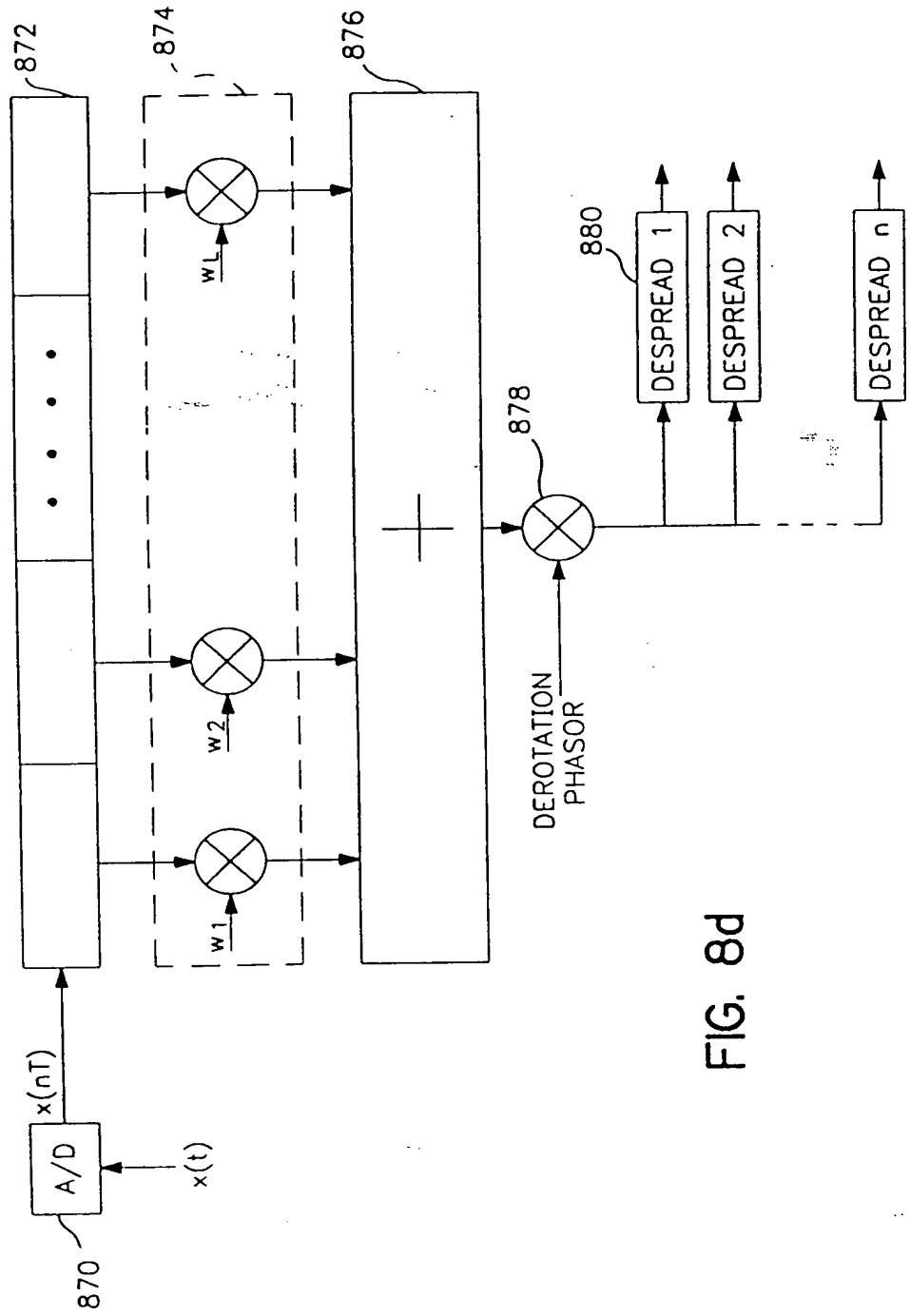

872
874
876
878
880
870
A/D
x(nT)
x(t)
W1
W2
WL
DEROTATION PHASOR
DESPREAD 1
DESPREAD 2
DESPREAD n

FIG. 8d

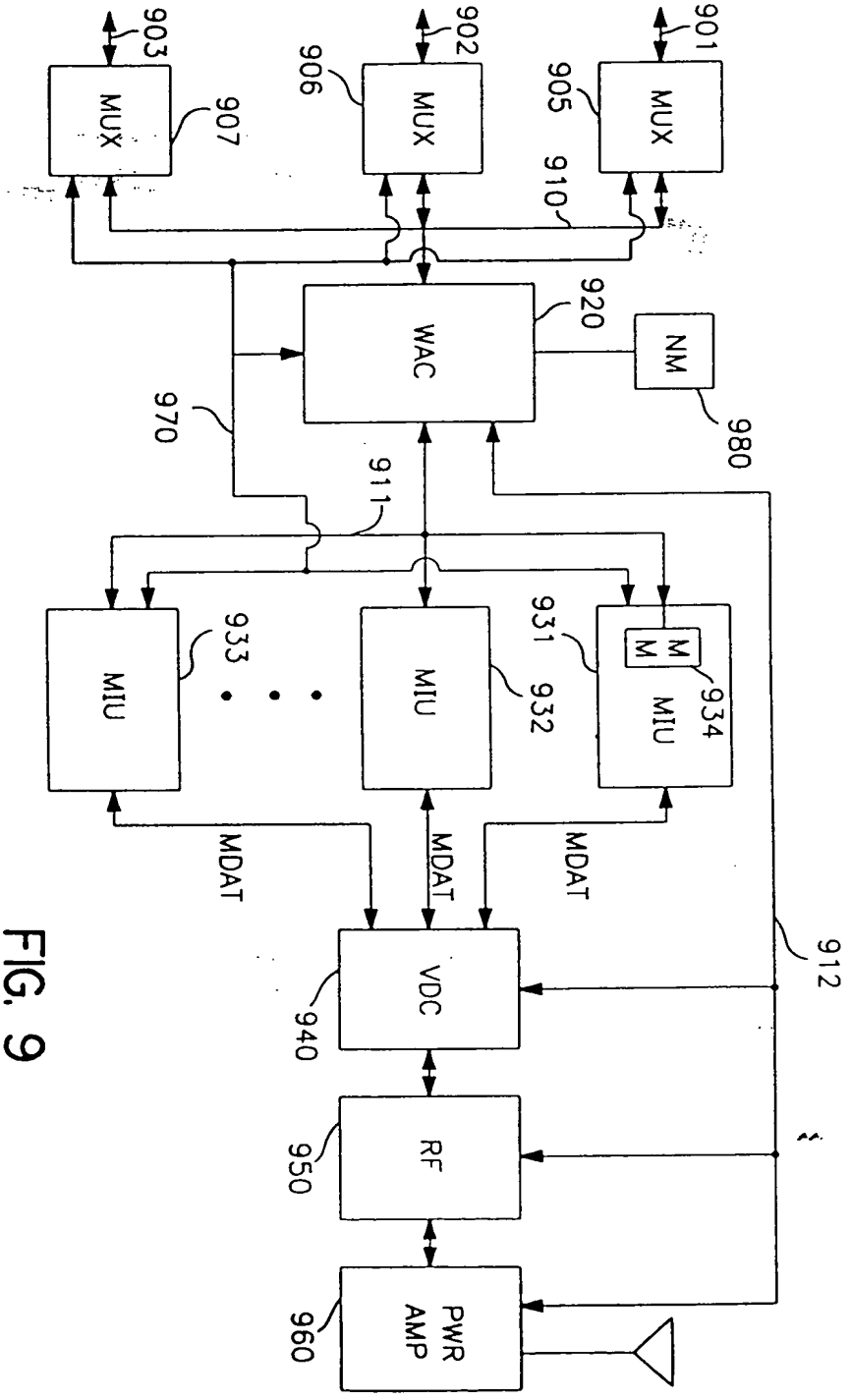

901
902
903
905
906
907
910
MUX
MUX
MUX
920
WAC
NM
980
970
911
912
931
932
933
934
MIU
MIU
MIU
MM
MDAT
MDAT
MDAT
940
VDC
950
RF
960
PWR
AMP

FIG. 9

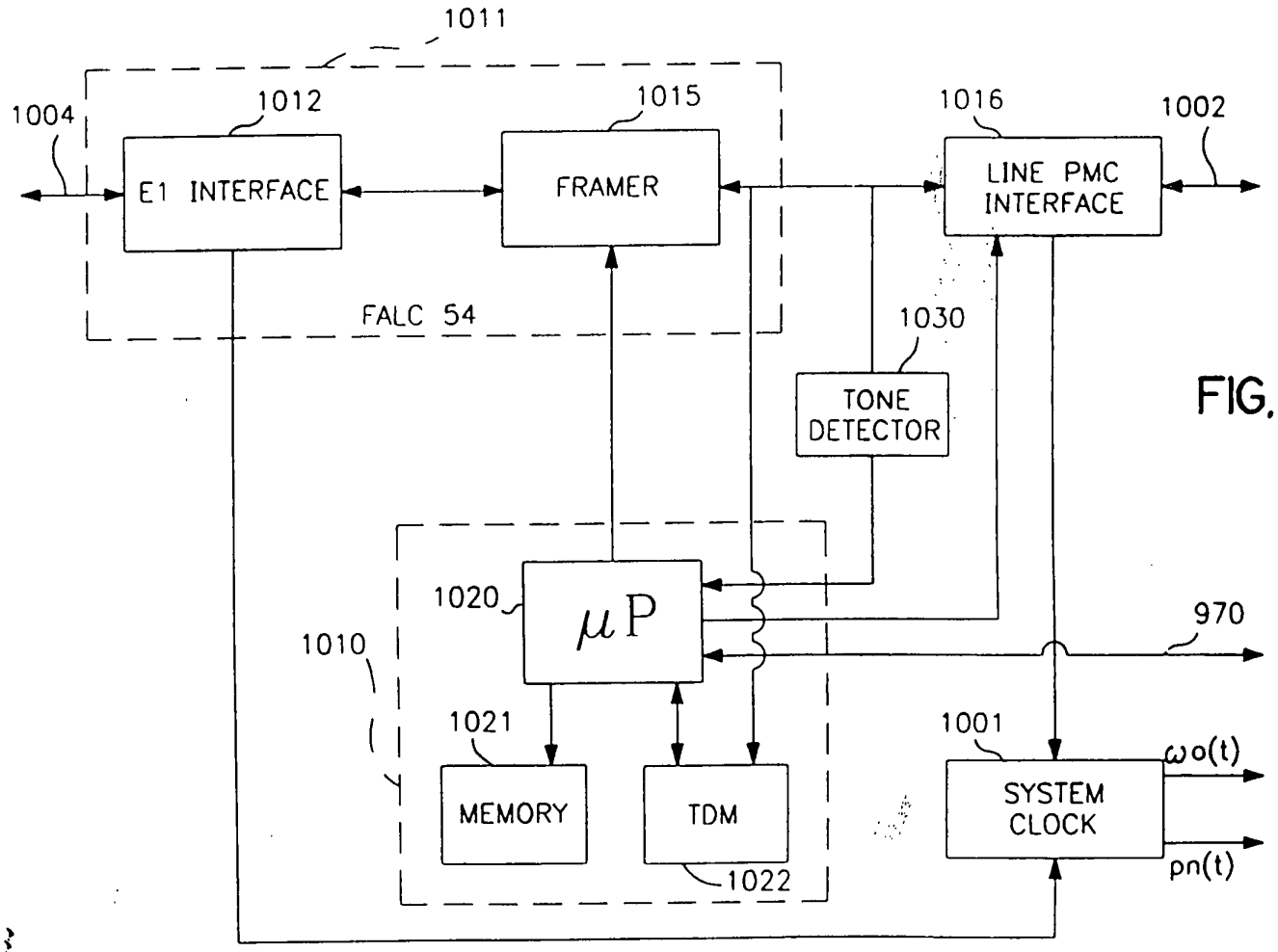

1011
1004
1012
1015
1016
1002
E1 INTERFACE
FRAMER
LINE PMC INTERFACE
FALC 54
1030
TONE DETECTOR
1020
μP
970
1010
1021
1001
ωo(t)
MEMORY
TDM
SYSTEM CLOCK
pn(t)
1022

FIG. 10

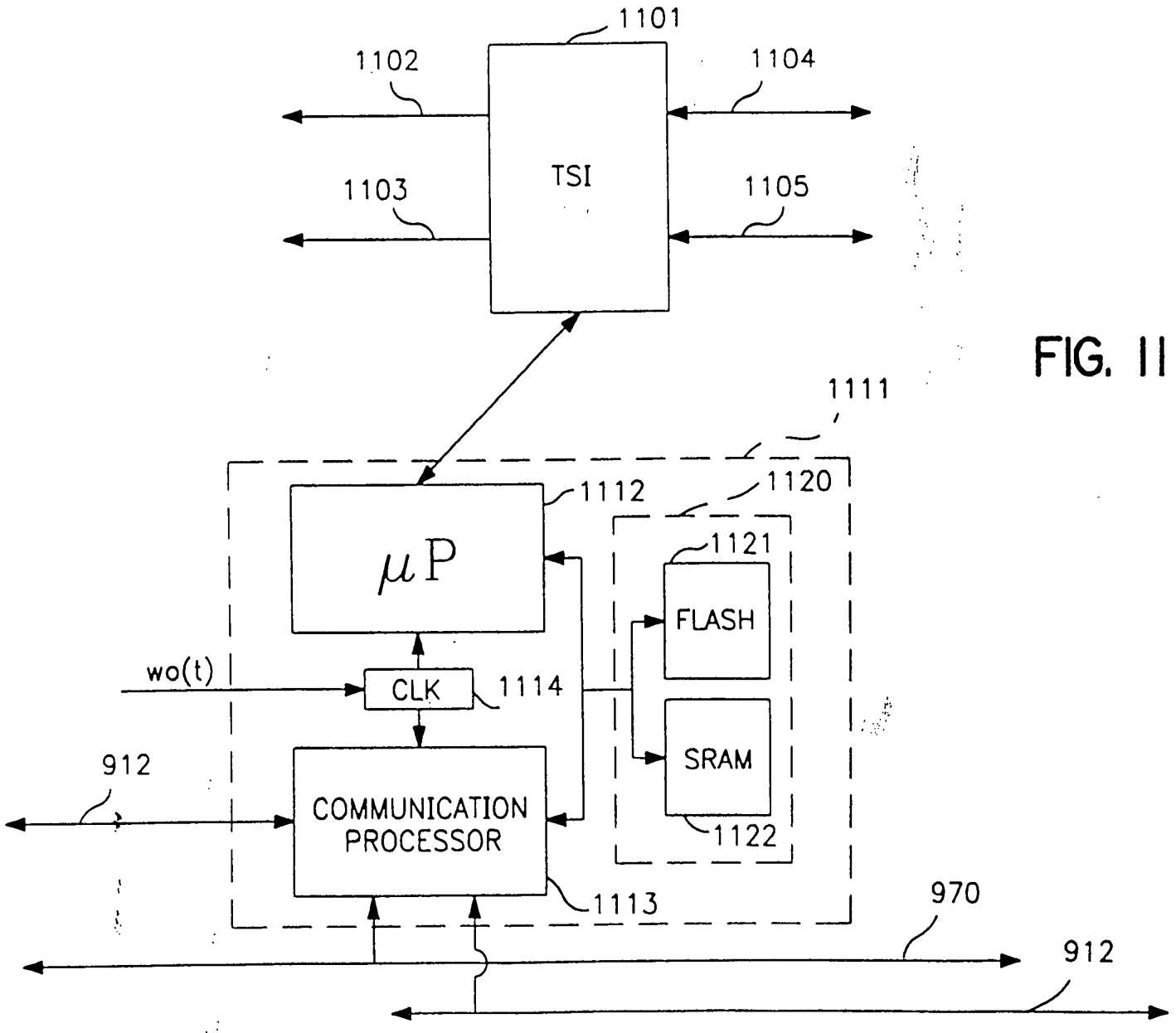

1101
1102
1104
TSI
1103
1105
1111
1112
1120
μP
1121
FLASH
wo(t)
CLK
1114
SRAM
912
COMMUNICATION PROCESSOR
1122
1113
970
912

FIG. 11

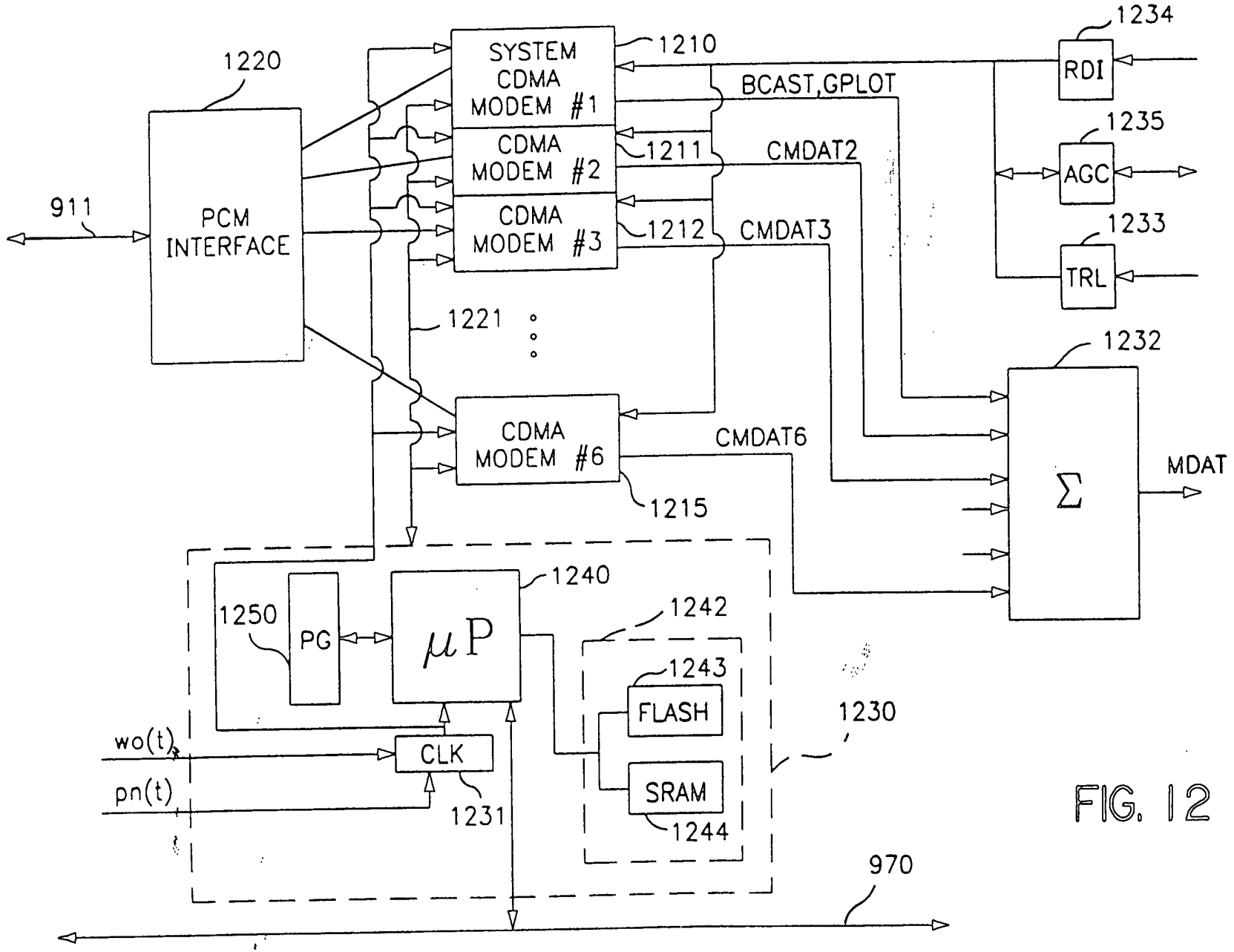

1234
RDI
1210
SYSTEM CDMA MODEM #1
BCAST,GPLOT
1220
1235
AGC
CDMA MODEM #2
1211
CMDAT2
911
PCM INTERFACE
CDMA MODEM #3
1212
CMDAT3
1233
TRL
1221
1232
CDMA MODEM #6
CMDAT6
MDAT
Σ
1215
1240
1250
PG
μP
1242
1243
FLASH
1230
wo(t)
CLK
SRAM
pn(t)
1231
1244
970

FIG. 12

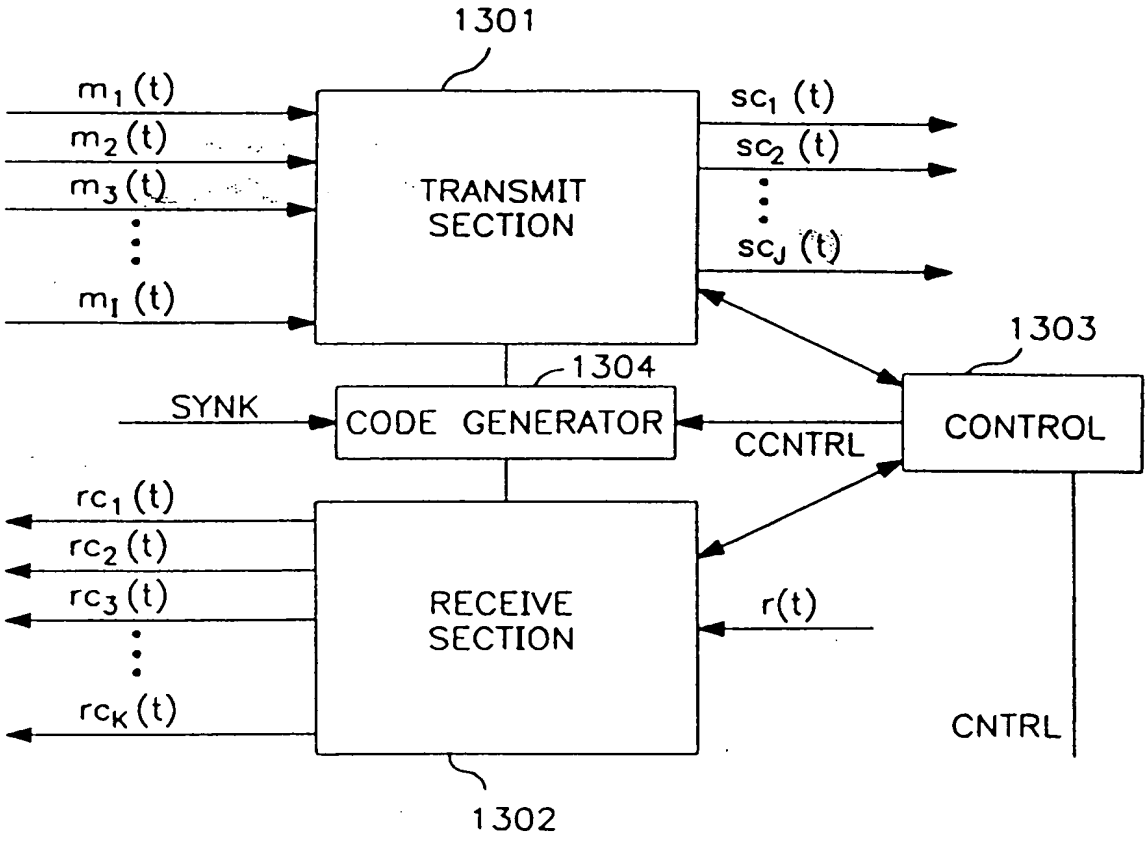

1301
$m_1(t)$
$m_2(t)$
$m_3(t)$
$m_I(t)$
TRANSMIT SECTION
$sc_1(t)$
$sc_2(t)$
$sc_J(t)$
1303
1304
SYNK
CODE GENERATOR
CCNTRL
CONTROL
$rc_1(t)$
$rc_2(t)$
$rc_3(t)$
$rc_K(t)$
RECEIVE SECTION
r(t)
CNTRL
1302

FIG. 13

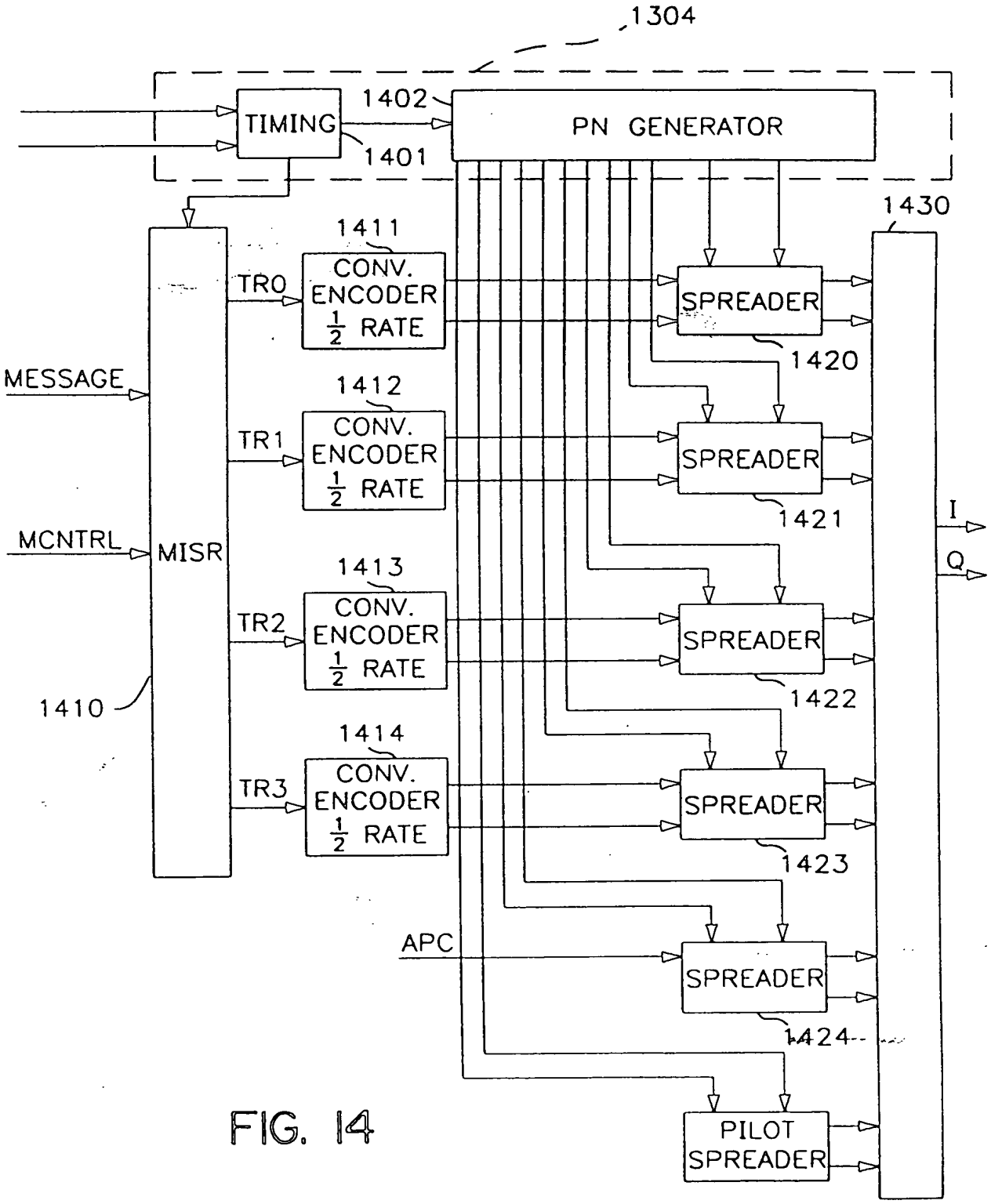

1304
TIMING
1402
1401
PN GENERATOR
1430
1411
CONV. ENCODER ½ RATE
TR0
SPREADER
1420
MESSAGE
1412
CONV. ENCODER ½ RATE
TR1
SPREADER
1421
I
MCNTRL
MISR
Q
1413
CONV. ENCODER ½ RATE
TR2
SPREADER
1422
1410
1414
CONV. ENCODER ½ RATE
TR3
SPREADER
1423
APC
SPREADER
1424
PILOT SPREADER

FIG. 14

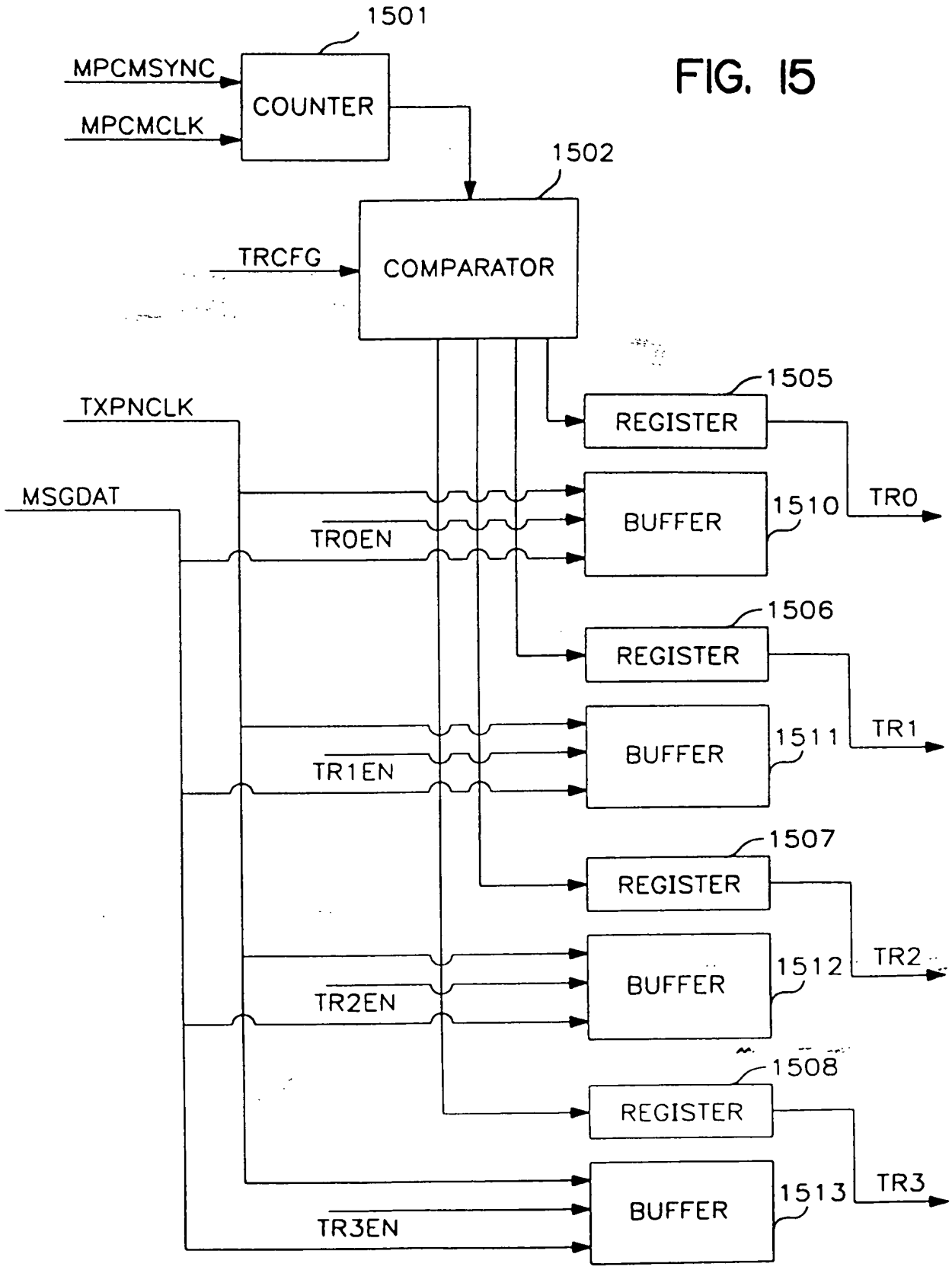

1501
MPCMSYNC
MPCMCLK
COUNTER
1502
TRCFG
COMPARATOR
TXPNCLK
MSGDAT
1505
REGISTER
BUFFER
1510
TR0
TR0EN
1506
REGISTER
BUFFER
1511
TR1
TR1EN
1507
REGISTER
BUFFER
1512
TR2
TR2EN
1508
REGISTER
BUFFER
1513
TR3
TR3EN

FIG. 15

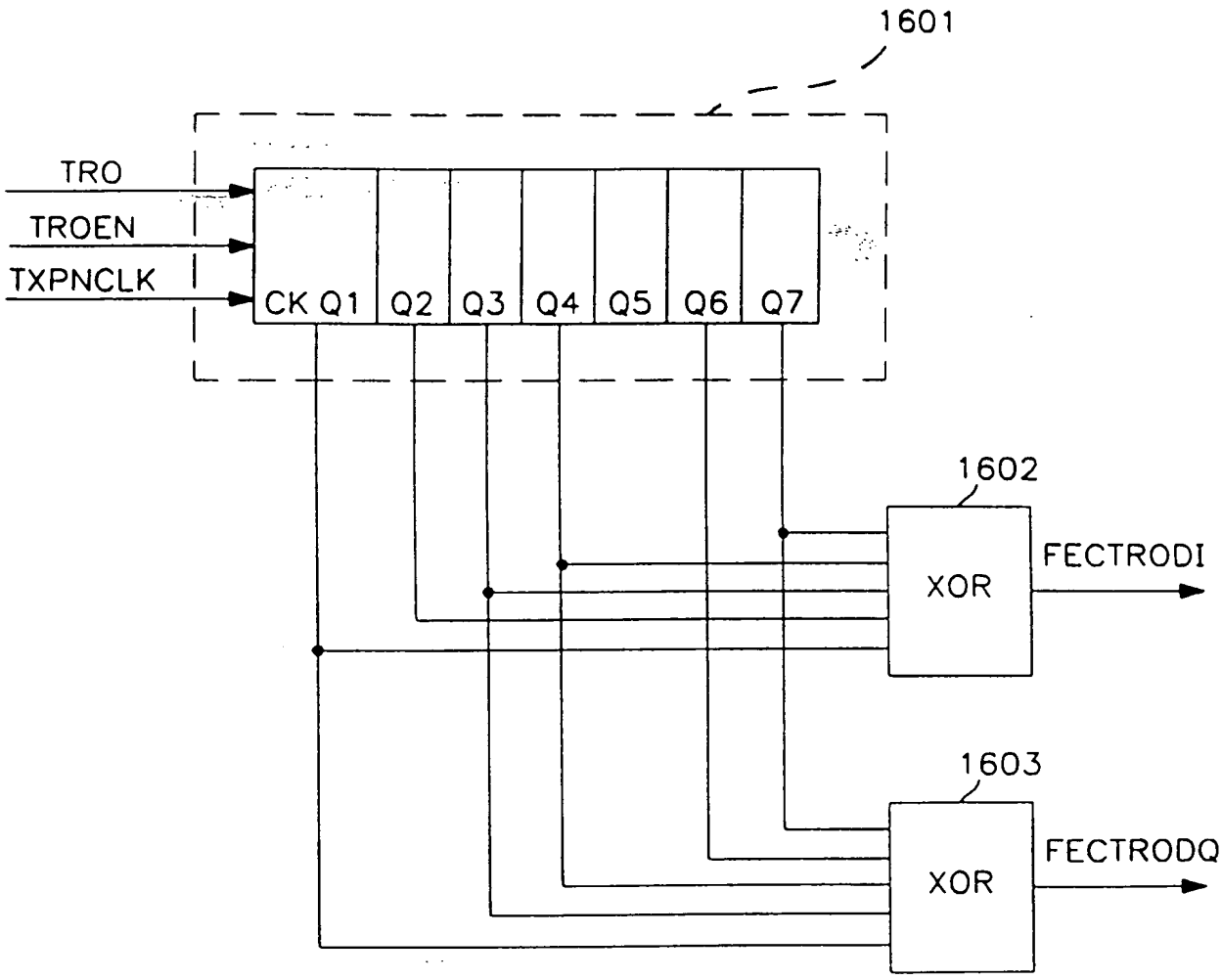

1601
TRO
TROEN
TXPNCLK
CK Q1
Q2
Q3
Q4
Q5
Q6
Q7
1602
XOR
FECTRODI
1603
XOR
FECTRODQ

FIG. 16

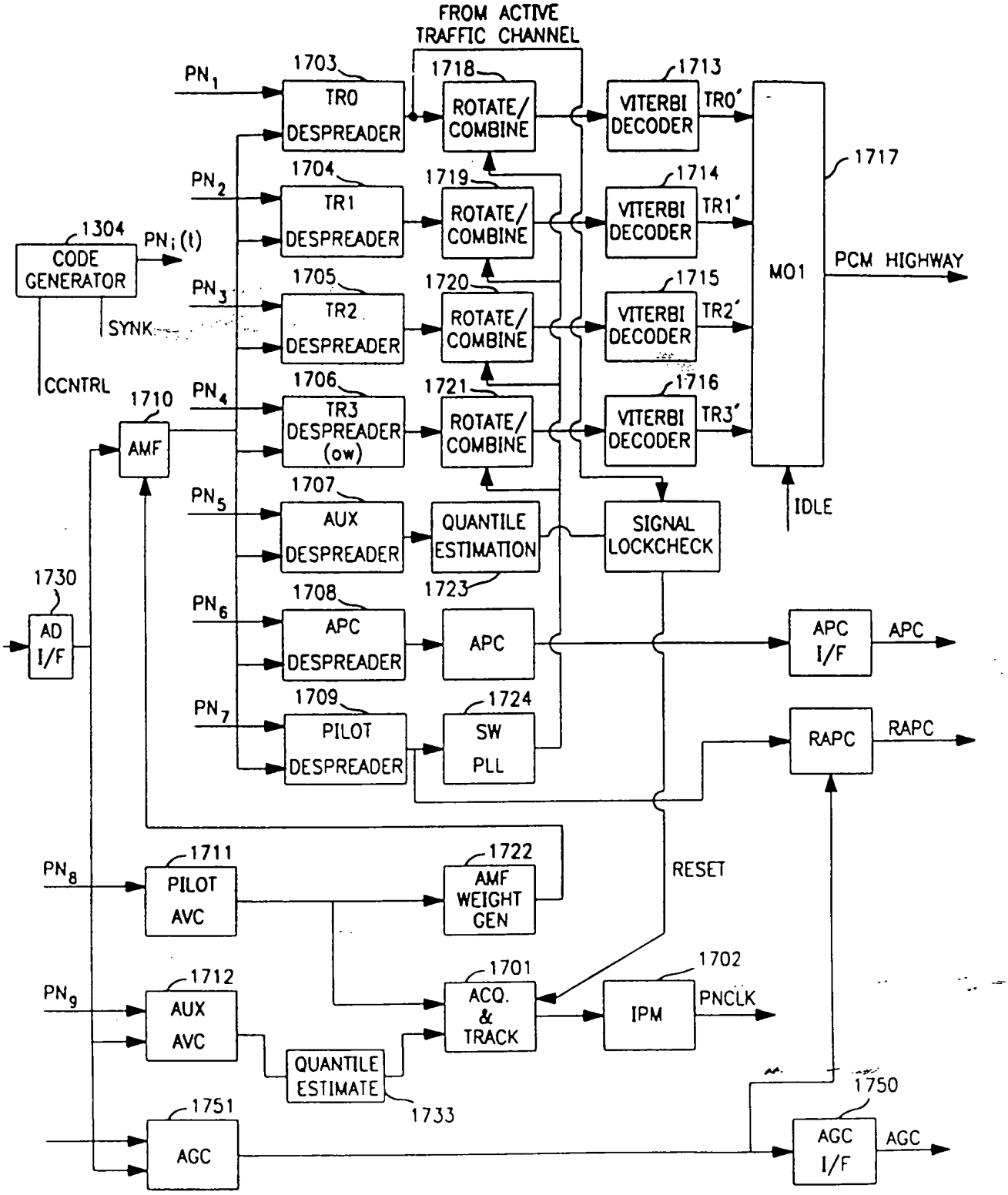

FROM ACTIVE TRAFFIC CHANNEL
PN1
1703
TR0 DESPREADER
1718
ROTATE/ COMBINE
1713
VITERBI DECODER
TR0'
1717
PN2
1704
TR1 DESPREADER
1719
ROTATE/ COMBINE
1714
VITERBI DECODER
TR1'
1304
CODE GENERATOR
PNi(t)
PN3
1705
TR2 DESPREADER
1720
ROTATE/ COMBINE
1715
VITERBI DECODER
TR2'
MOI
PCM HIGHWAY
SYNK
CCNTRL
1710
PN4
1706
TR3 DESPREADER (ow)
1721
ROTATE/ COMBINE
1716
VITERBI DECODER
TR3'
AMF
PN5
1707
AUX DESPREADER
QUANTILE ESTIMATION
SIGNAL LOCKCHECK
IDLE
1730
1723
PN6
1708
APC DESPREADER
APC
APC I/F
APC
AD I/F
PN7
1709
PILOT DESPREADER
1724
SW PLL
RAPC
RAPC
RESET
PN8
1711
PILOT AVC
1722
AMF WEIGHT GEN
1701
1702
PN9
1712
AUX AVC
ACQ. & TRACK
IPM
PNCLK
QUANTILE ESTIMATE
1733
1750
1751
AGC
AGC I/F
AGC

FIG. 17

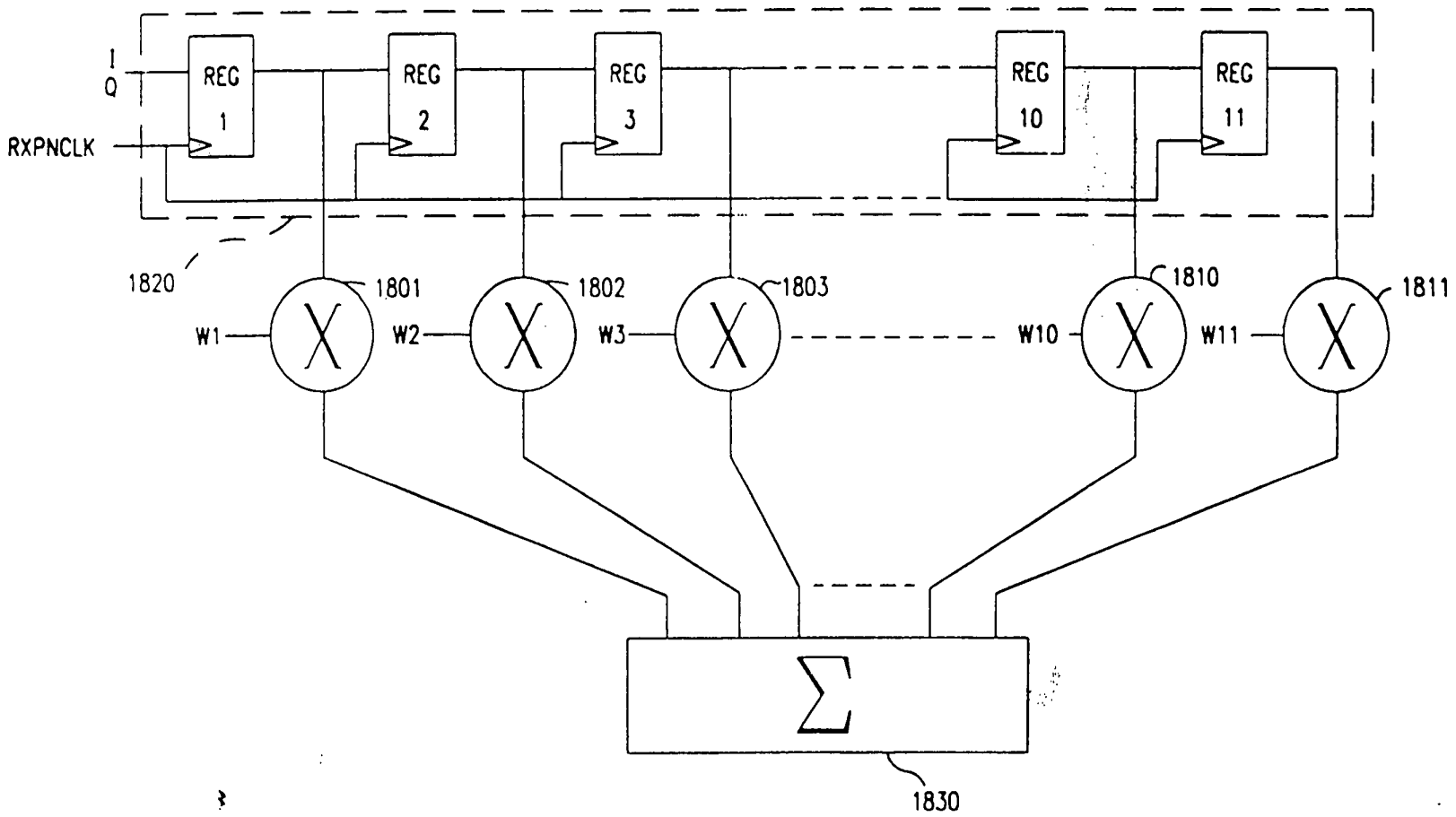

I
Q
RXPNCLK
REG 1
REG 2
REG 3
REG 10
REG 11
1820
1801
1802
1803
1810
1811
W1
W2
W3
W10
W11
Σ
1830

FIG. 18

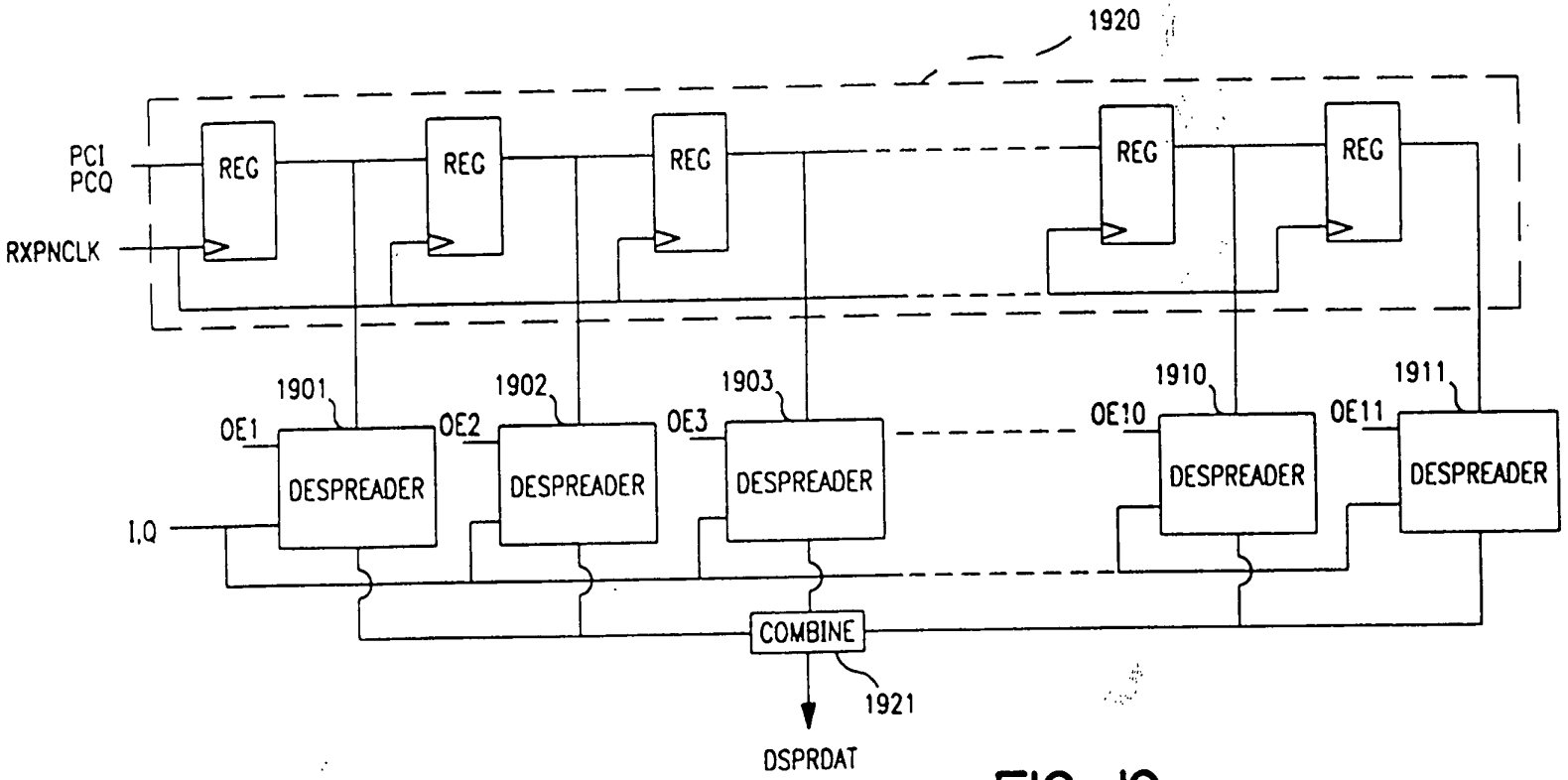

1920
PCI
PCQ
RXPNCLK
REG
REG
REG
REG
REG
1901
1902
1903
1910
1911
OE1
OE2
OE3
OE10
OE11
DESPREADER
DESPREADER
DESPREADER
DESPREADER
DESPREADER
I,Q
COMBINE
1921
DSPRDAT

FIG. 19

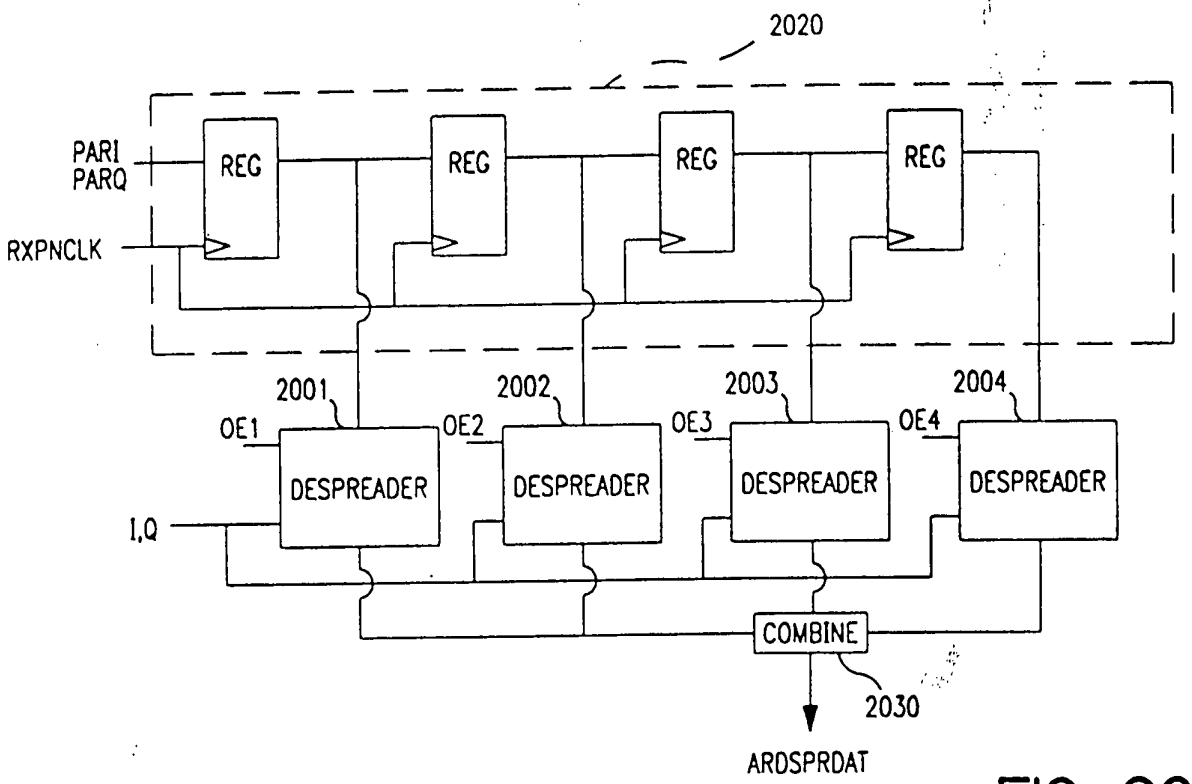

2020
PARI
PARQ
RXPNCLK
REG
REG
REG
REG
2001
2002
2003
2004
OE1
OE2
OE3
OE4
DESPREADER
DESPREADER
DESPREADER
DESPREADER
I,Q
COMBINE
2030
ARDSPRDAT

FIG. 20

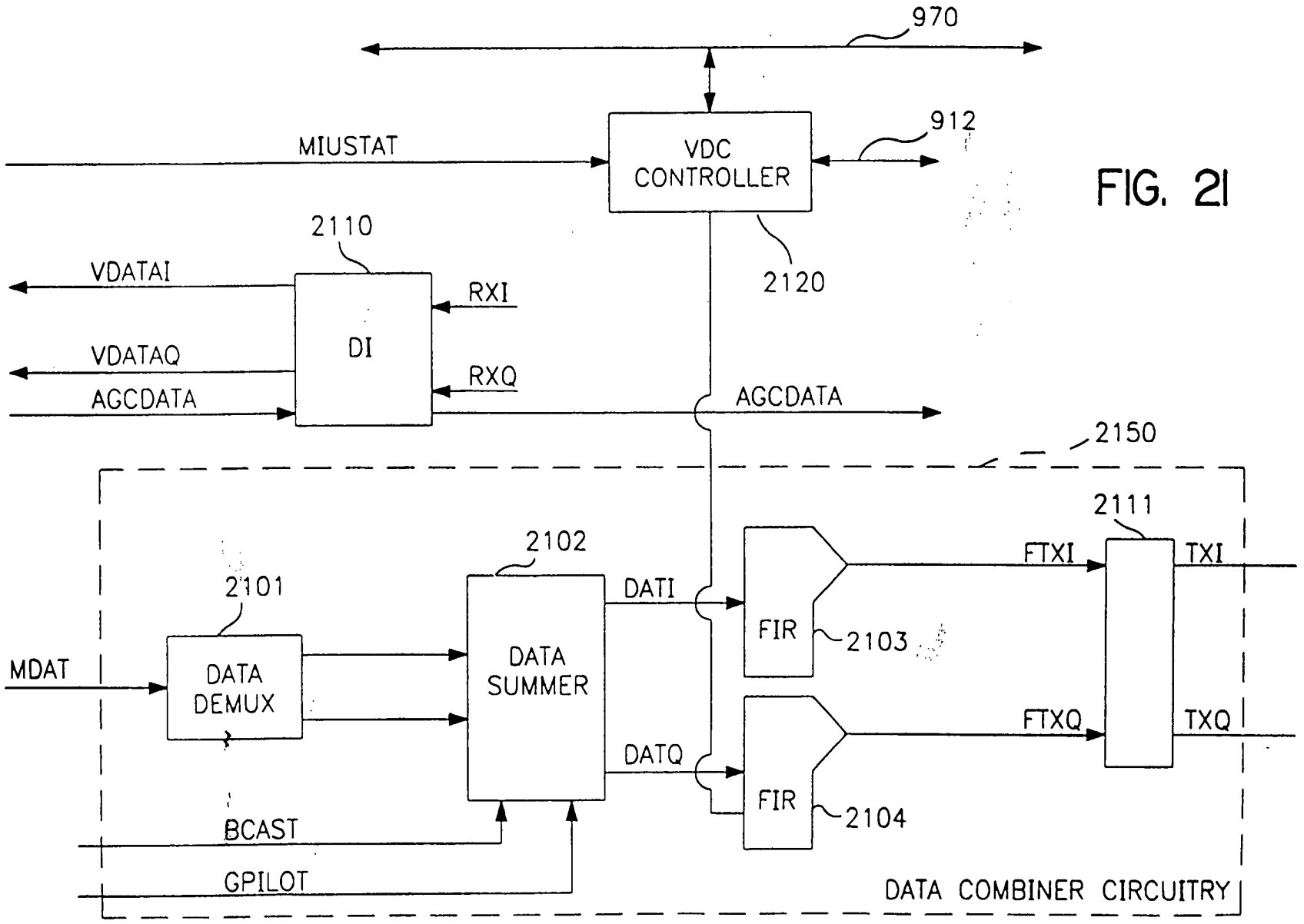

970
912
MIUSTAT
VDC CONTROLLER
2110
VDATAI
RXI
DI
VDATAQ
RXQ
AGCDATA
2120
AGCDATA
2150
2111
2102
2101
DATI
FTXI
TXI
FIR
2103
MDAT
DATA DEMUX
DATA SUMMER
DATQ
FTXQ
TXQ
FIR
2104
BCAST
GPILOT
DATA COMBINER CIRCUITRY

FIG. 21

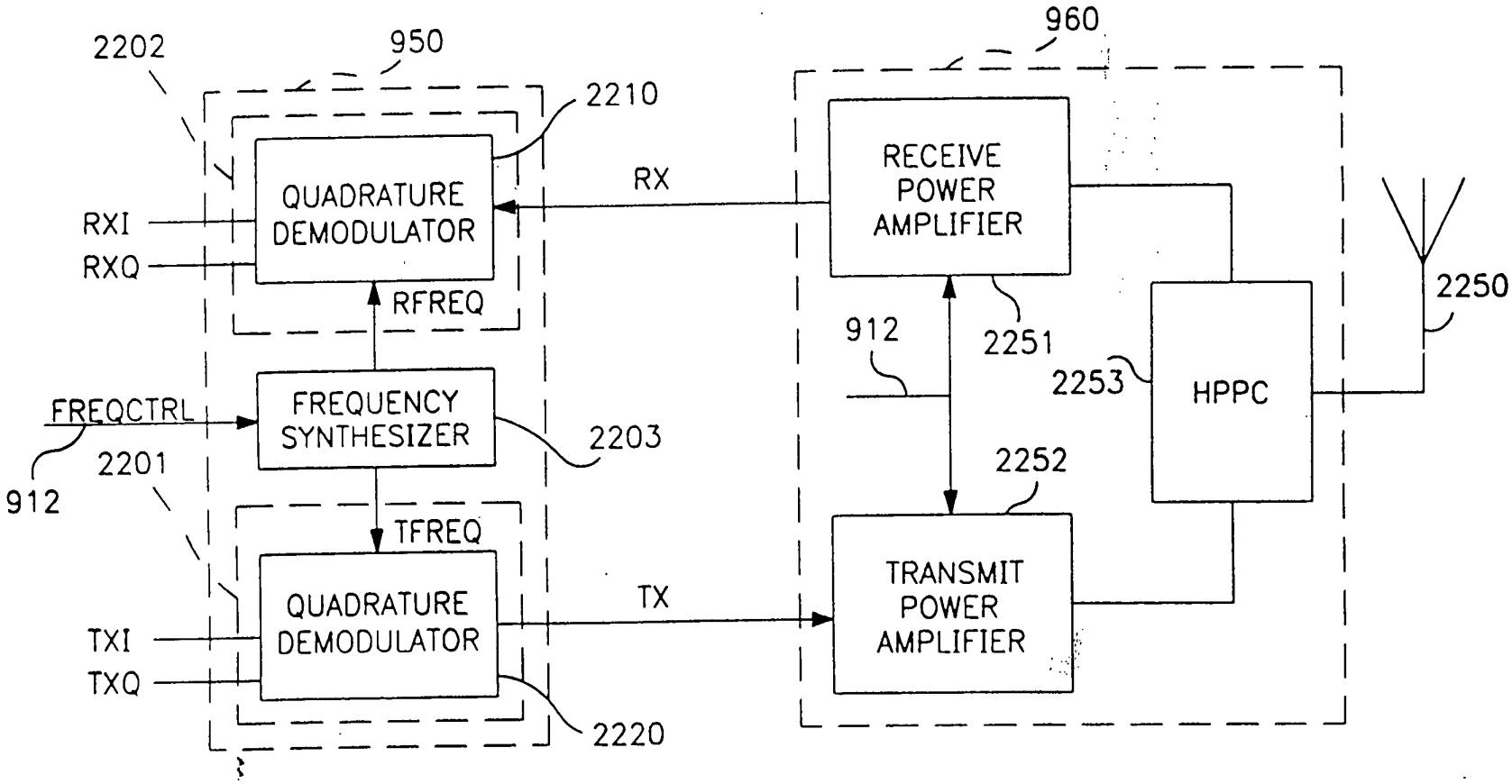

2202
950
960
2210
QUADRATURE DEMODULATOR
RXI
RXQ
RX
RECEIVE POWER AMPLIFIER
RFREQ
912
2251
2253
HPPC
2250
FREQCTRL
FREQUENCY SYNTHESIZER
2203
912
2201
2252
TFREQ
QUADRATURE DEMODULATOR
TX
TRANSMIT POWER AMPLIFIER
TXI
TXQ
2220

FIG. 22

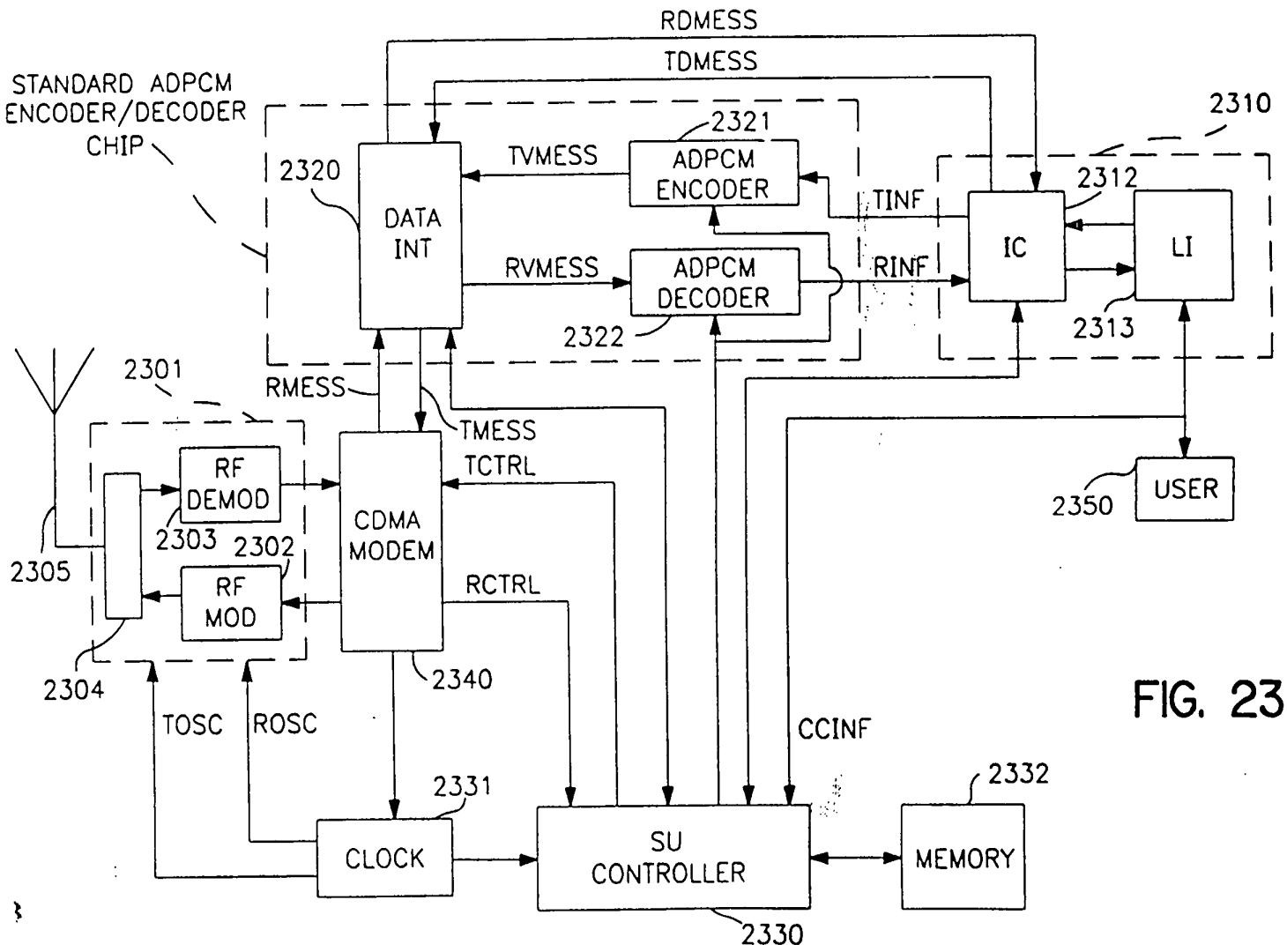

RDMESS
TDMESS
STANDARD ADPCM ENCODER/DECODER CHIP
2310
2321
2320
TVMESS
ADPCM ENCODER
2312
DATA INT
TINF
IC
LI
RVMESS
ADPCM DECODER
RINF
2322
2313
2301
RMESS
TMESS
TCTRL
RF DEMOD
CDMA MODEM
2350
USER
2303
2302
2305
RF MOD
RCTRL
2304
2340
TOSC
ROSC
CCINF
2331
2332
CLOCK
SU CONTROLLER
MEMORY
2330

FIG. 23

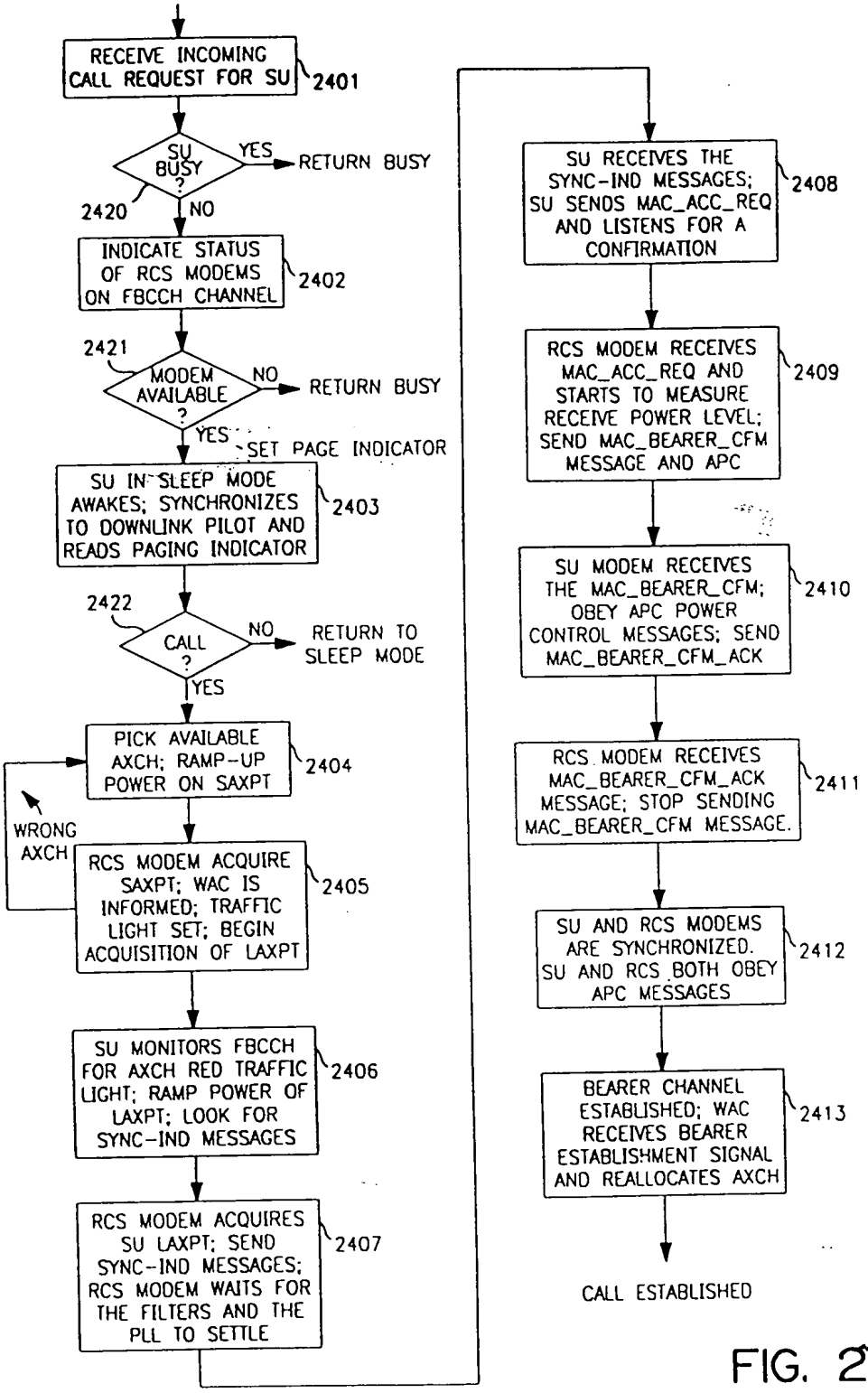

RECEIVE INCOMING CALL REQUEST FOR SU
2401
SU BUSY ?
YES
RETURN BUSY
2420
NO
INDICATE STATUS OF RCS MODEMS ON FBCCH CHANNEL
2402
2421
MODEM AVAILABLE ?
NO
RETURN BUSY
YES
SET PAGE INDICATOR
SU IN SLEEP MODE AWAKES; SYNCHRONIZES TO DOWNLINK PILOT AND READS PAGING INDICATOR
2403
2422
CALL ?
NO
RETURN TO SLEEP MODE
YES
PICK AVAILABLE AXCH; RAMP-UP POWER ON SAXPT
2404
WRONG AXCH
RCS MODEM ACQUIRE SAXPT; WAC IS INFORMED; TRAFFIC LIGHT SET; BEGIN ACQUISITION OF LAXPT
2405
SU MONITORS FBCCH FOR AXCH RED TRAFFIC LIGHT; RAMP POWER OF LAXPT; LOOK FOR SYNC-IND MESSAGES
2406
RCS MODEM ACQUIRES SU LAXPT; SEND SYNC-IND MESSAGES; RCS MODEM WAITS FOR THE FILTERS AND THE PLL TO SETTLE
2407
SU RECEIVES THE SYNC-IND MESSAGES; SU SENDS MAC_ACC_REQ AND LISTENS FOR A CONFIRMATION
2408
RCS MODEM RECEIVES MAC_ACC_REQ AND STARTS TO MEASURE RECEIVE POWER LEVEL; SEND MAC_BEARER_CFM MESSAGE AND APC
2409
SU MODEM RECEIVES THE MAC_BEARER_CFM; OBEY APC POWER CONTROL MESSAGES; SEND MAC_BEARER_CFM_ACK
2410
RCS MODEM RECEIVES MAC_BEARER_CFM_ACK MESSAGE; STOP SENDING MAC_BEARER_CFM MESSAGE.
2411
SU AND RCS MODEMS ARE SYNCHRONIZED. SU AND RCS BOTH OBEY APC MESSAGES
2412
BEARER CHANNEL ESTABLISHED; WAC RECEIVES BEARER ESTABLISHMENT SIGNAL AND REALLOCATES AXCH
2413
CALL ESTABLISHED

FIG. 24

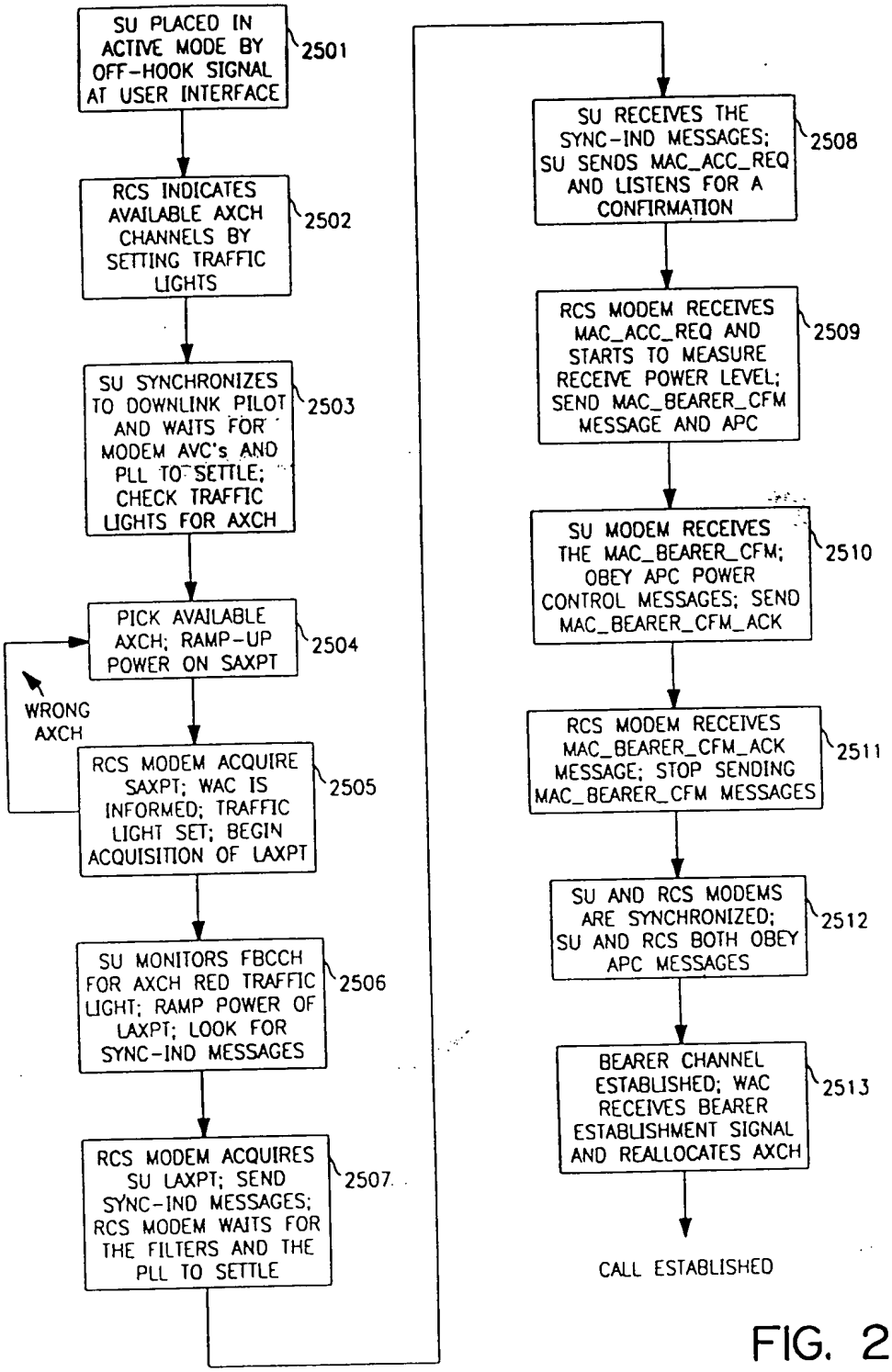

SU PLACED IN ACTIVE MODE BY OFF-HOOK SIGNAL AT USER INTERFACE
2501
RCS INDICATES AVAILABLE AXCH CHANNELS BY SETTING TRAFFIC LIGHTS
2502
SU SYNCHRONIZES TO DOWNLINK PILOT AND WAITS FOR MODEM AVC's AND PLL TO SETTLE; CHECK TRAFFIC LIGHTS FOR AXCH
2503
PICK AVAILABLE AXCH; RAMP-UP POWER ON SAXPT
2504
WRONG AXCH
RCS MODEM ACQUIRE SAXPT; WAC IS INFORMED; TRAFFIC LIGHT SET; BEGIN ACQUISITION OF LAXPT
2505
SU MONITORS FBCCH FOR AXCH RED TRAFFIC LIGHT; RAMP POWER OF LAXPT; LOOK FOR SYNC-IND MESSAGES
2506
RCS MODEM ACQUIRES SU LAXPT; SEND SYNC-IND MESSAGES; RCS MODEM WAITS FOR THE FILTERS AND THE PLL TO SETTLE
2507
SU RECEIVES THE SYNC-IND MESSAGES; SU SENDS MAC_ACC_REQ AND LISTENS FOR A CONFIRMATION
2508
RCS MODEM RECEIVES MAC_ACC_REQ AND STARTS TO MEASURE RECEIVE POWER LEVEL; SEND MAC_BEARER_CFM MESSAGE AND APC
2509
SU MODEM RECEIVES THE MAC_BEARER_CFM; OBEY APC POWER CONTROL MESSAGES; SEND MAC_BEARER_CFM_ACK
2510
RCS MODEM RECEIVES MAC_BEARER_CFM_ACK MESSAGE; STOP SENDING MAC_BEARER_CFM MESSAGES
2511
SU AND RCS MODEMS ARE SYNCHRONIZED; SU AND RCS BOTH OBEY APC MESSAGES
2512
BEARER CHANNEL ESTABLISHED; WAC RECEIVES BEARER ESTABLISHMENT SIGNAL AND REALLOCATES AXCH
2513
CALL ESTABLISHED

FIG. 25

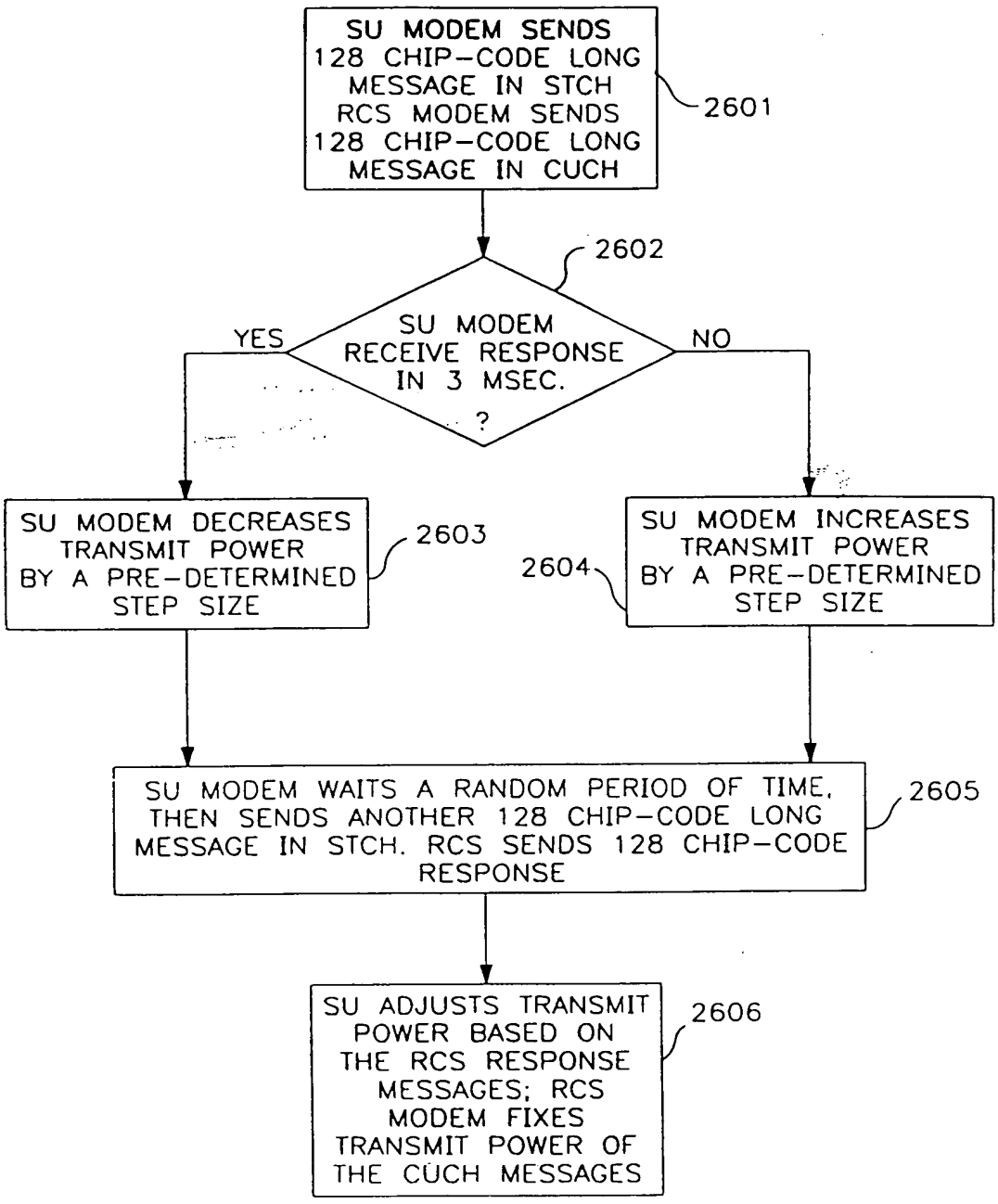

SU MODEM SENDS 128 CHIP-CODE LONG MESSAGE IN STCH RCS MODEM SENDS 128 CHIP-CODE LONG MESSAGE IN CUCH
2601
2602
SU MODEM RECEIVE RESPONSE IN 3 MSEC. ?
YES
NO
SU MODEM DECREASES TRANSMIT POWER BY A PRE-DETERMINED STEP SIZE
2603
SU MODEM INCREASES TRANSMIT POWER BY A PRE-DETERMINED STEP SIZE
2604
SU MODEM WAITS A RANDOM PERIOD OF TIME, THEN SENDS ANOTHER 128 CHIP-CODE LONG MESSAGE IN STCH. RCS SENDS 128 CHIP-CODE RESPONSE
2605
SU ADJUSTS TRANSMIT POWER BASED ON THE RCS RESPONSE MESSAGES; RCS MODEM FIXES TRANSMIT POWER OF THE CUCH MESSAGES
2606

FIG. 26

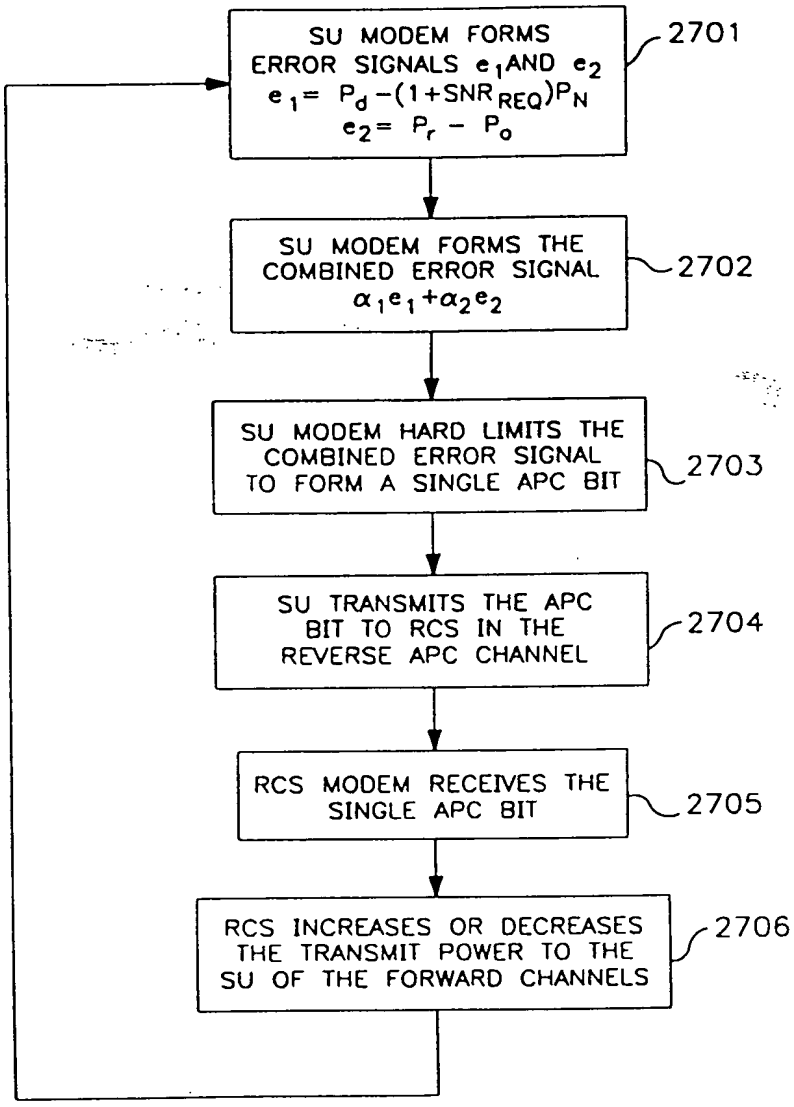

SU MODEM FORMS ERROR SIGNALS e_1 AND e_2
$e_1 = P_d - (1+SNR_{REQ})P_N$
$e_2 = P_r - P_o$
2701
SU MODEM FORMS THE COMBINED ERROR SIGNAL
$\alpha_1 e_1 + \alpha_2 e_2$
2702
SU MODEM HARD LIMITS THE COMBINED ERROR SIGNAL TO FORM A SINGLE APC BIT
2703
SU TRANSMITS THE APC BIT TO RCS IN THE REVERSE APC CHANNEL
2704
RCS MODEM RECEIVES THE SINGLE APC BIT
2705
RCS INCREASES OR DECREASES THE TRANSMIT POWER TO THE SU OF THE FORWARD CHANNELS
2706

FIG. 27

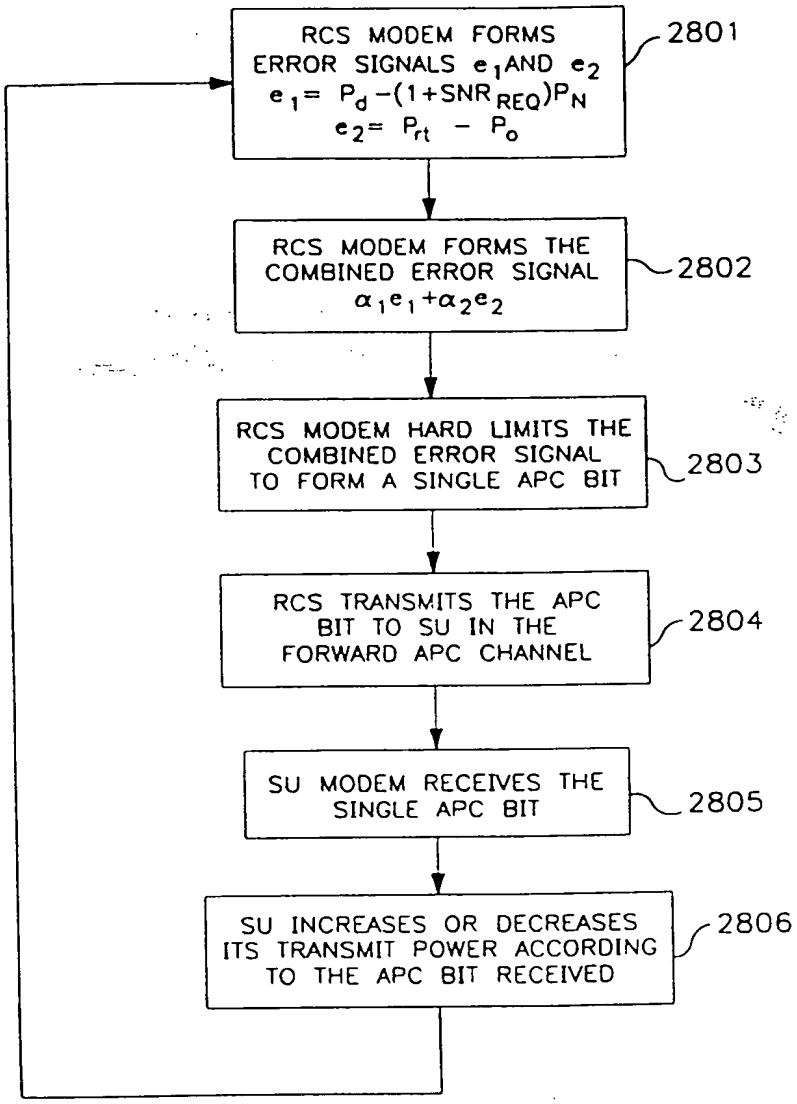

RCS MODEM FORMS ERROR SIGNALS e_1 AND e_2
$e_1 = P_d - (1+SNR_{REQ})P_N$
$e_2 = P_{rt} - P_o$
2801
RCS MODEM FORMS THE COMBINED ERROR SIGNAL
$\alpha_1 e_1 + \alpha_2 e_2$
2802
RCS MODEM HARD LIMITS THE COMBINED ERROR SIGNAL TO FORM A SINGLE APC BIT
2803
RCS TRANSMITS THE APC BIT TO SU IN THE FORWARD APC CHANNEL
2804
SU MODEM RECEIVES THE SINGLE APC BIT
2805
SU INCREASES OR DECREASES ITS TRANSMIT POWER ACCORDING TO THE APC BIT RECEIVED
2806

FIG. 28

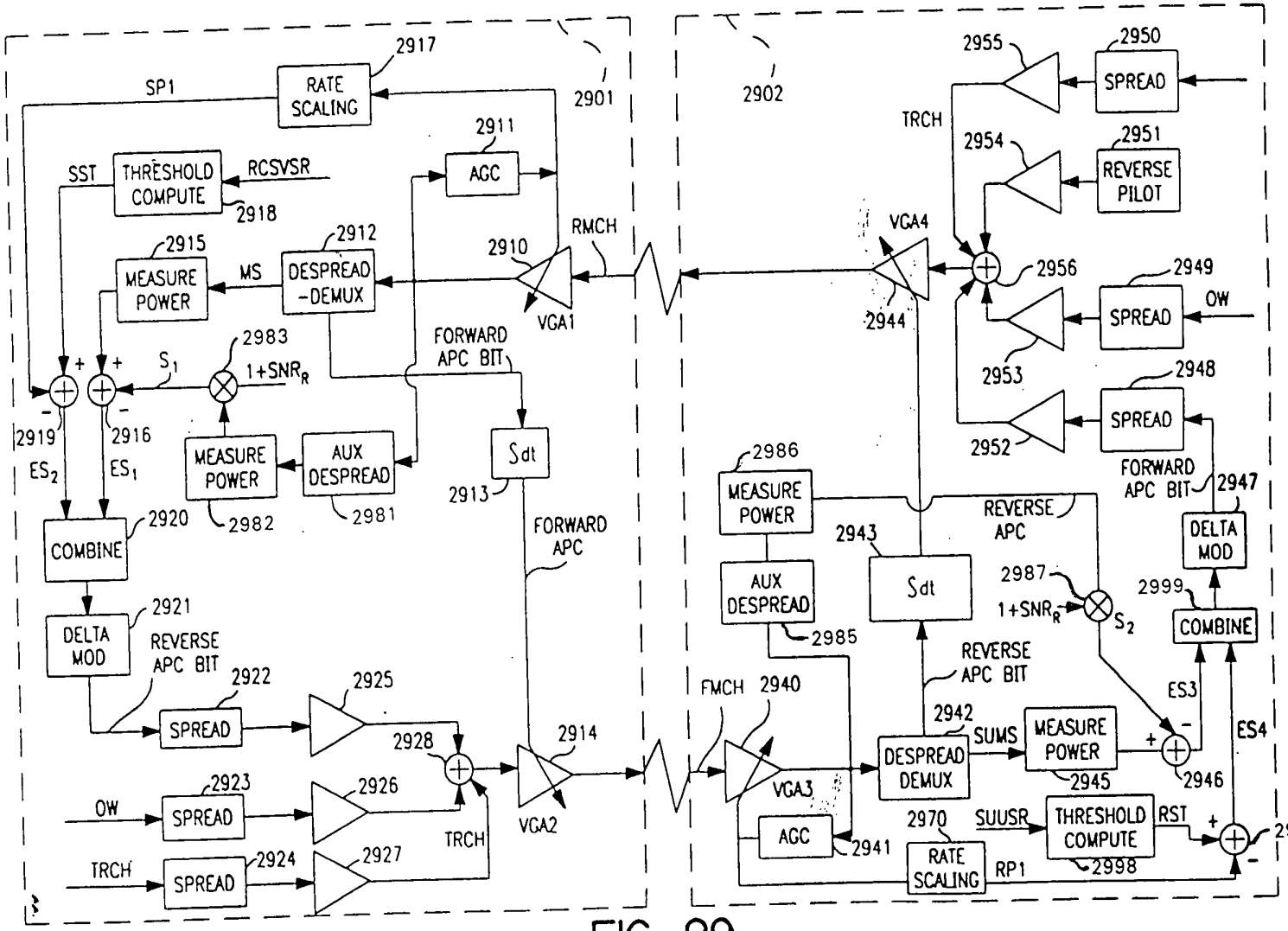

2901
2902
RATE SCALING
2917
SP1
THRESHOLD COMPUTE
SST
RCSVSR
2918
AGC
2911
MEASURE POWER
2915
MS
DESPREAD -DEMUX
2912
RMCH
2910
VGA1
2983
1+SNR_R
S_1
FORWARD APC BIT
2919
2916
ES_2
ES_1
MEASURE POWER
AUX DESPREAD
2982
2981
Sdt
2913
COMBINE
2920
FORWARD APC
DELTA MOD
2921
REVERSE APC BIT
SPREAD
2922
2925
2928
2914
OW
2923
2926
TRCH
SPREAD
2924
2927
VGA2
2955
2950
SPREAD
TRCH
2954
2951
REVERSE PILOT
VGA4
2956
2949
SPREAD
OW
2944
2953
2948
SPREAD
2952
FORWARD APC BIT
2947
DELTA MOD
2986
MEASURE POWER
REVERSE APC
2943
AUX DESPREAD
Sdt
2987
1+SNR_R
S_2
2999
COMBINE
2985
REVERSE APC BIT
FMCH
2940
ES3
2942
SUMS
MEASURE POWER
ES4
DESPREAD DEMUX
2945
2946
VGA3
2970
SUUSR
THRESHOLD COMPUTE
RST
2994
AGC
2941
RATE SCALING
RP1
2998

FIG. 29

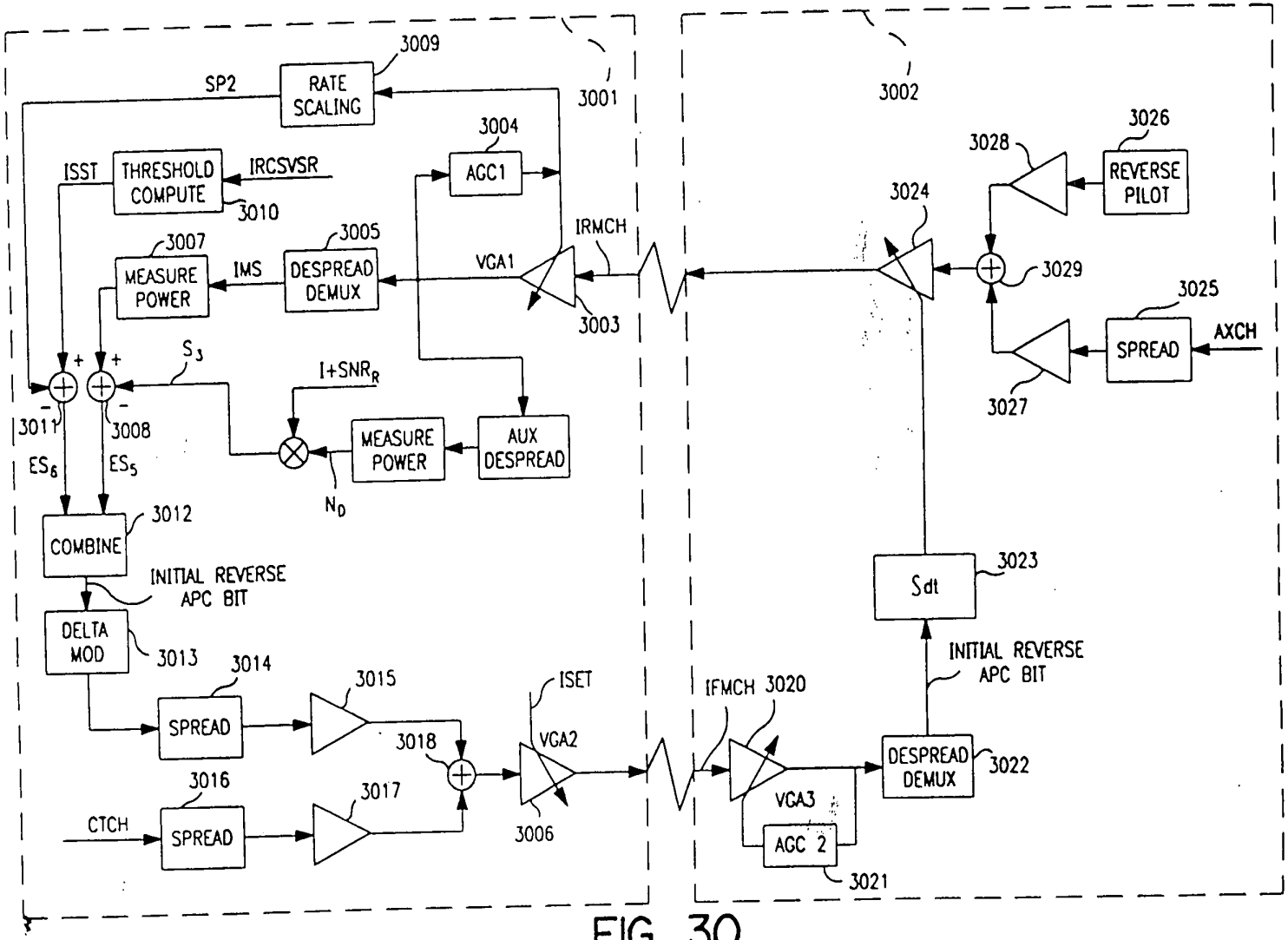

3001
3002
3009
RATE SCALING
SP2
3004
AGC1
ISST
THRESHOLD COMPUTE
IRCSVSR
3010
3007
MEASURE POWER
IMS
3005
DESPREAD DEMUX
VGA1
IRMCH
3003
3024
3028
3026
REVERSE PILOT
3029
3025
SPREAD
AXCH
3027
S_3
$I+SNR_R$
3011
3008
ES_6
ES_5
MEASURE POWER
AUX DESPREAD
N_0
3012
COMBINE
INITIAL REVERSE APC BIT
DELTA MOD
3013
3014
SPREAD
3015
3018
ISET
VGA2
3006
3016
CTCH
SPREAD
3017
IFMCH 3020
VGA3
AGC 2
3021
3023
Sdt
INITIAL REVERSE APC BIT
DESPREAD DEMUX
3022

FIG. 30

FIG. 31

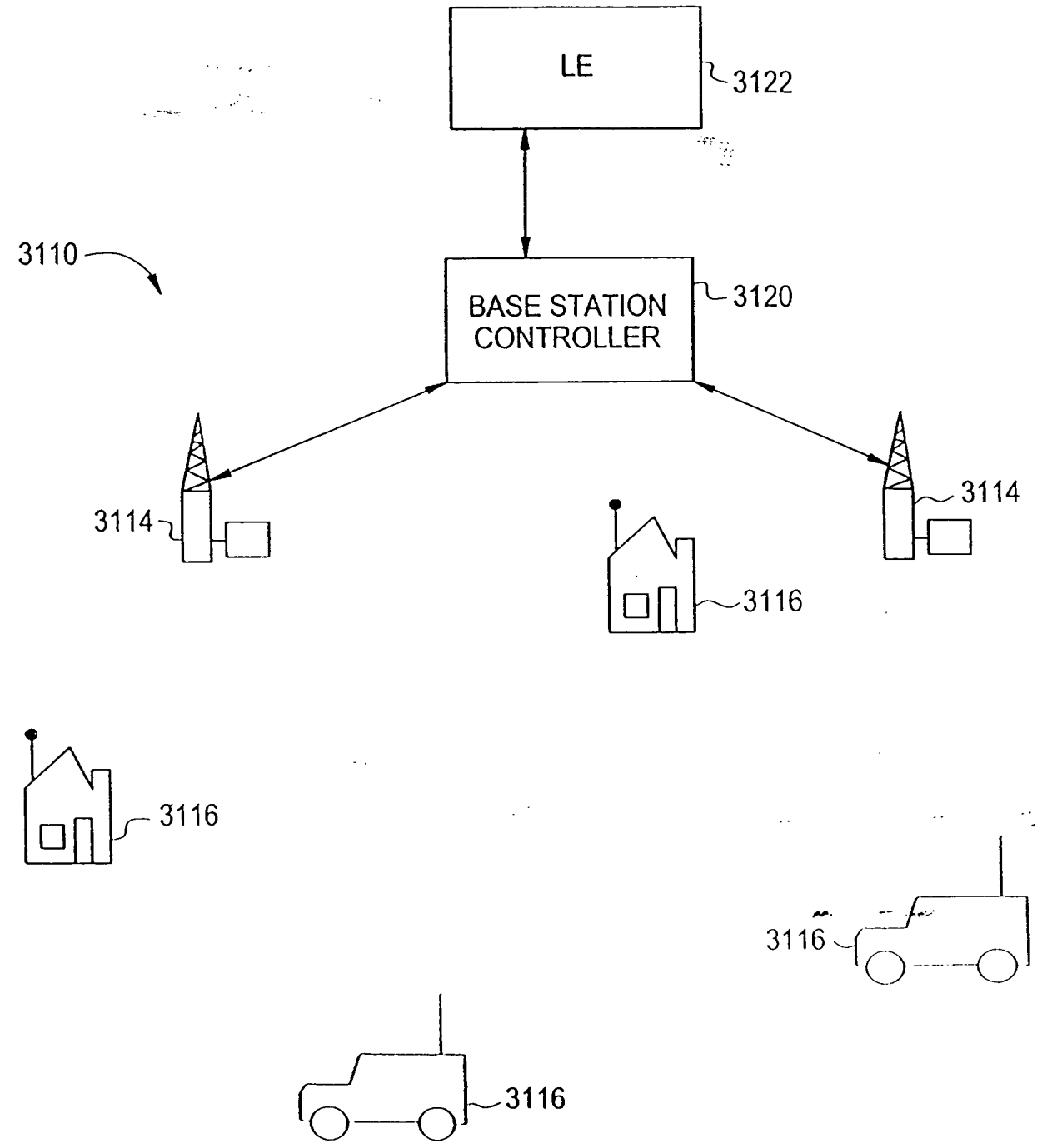

LE
3122
3110
BASE STATION CONTROLLER
3120
3114
3114
3116
3116
3116
3116

FIG. 32

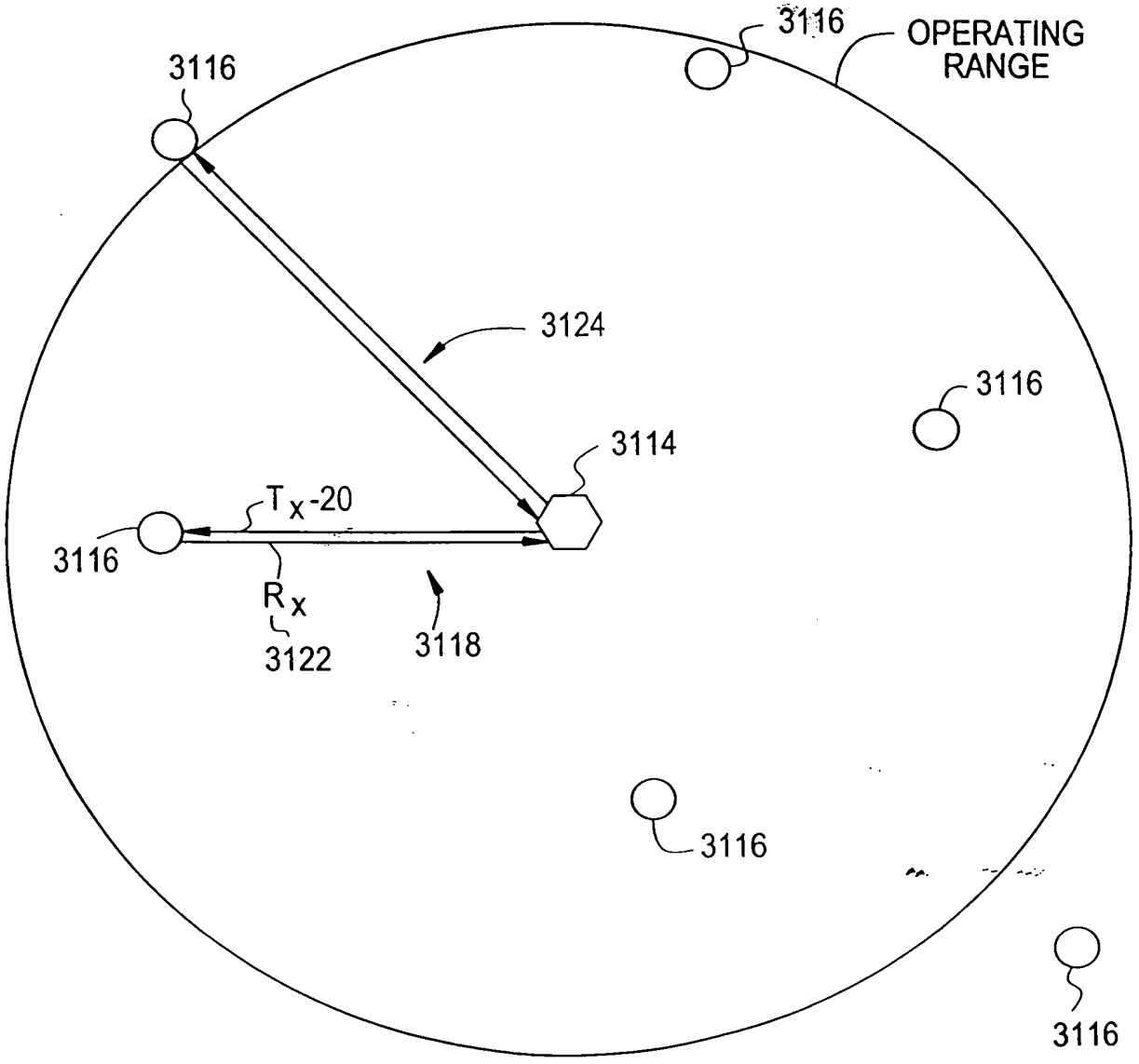

3116
3116
OPERATING RANGE
3124
3116
3114
Tx-20
3116
Rx
3122
3118
3116
3116

FIG. 33

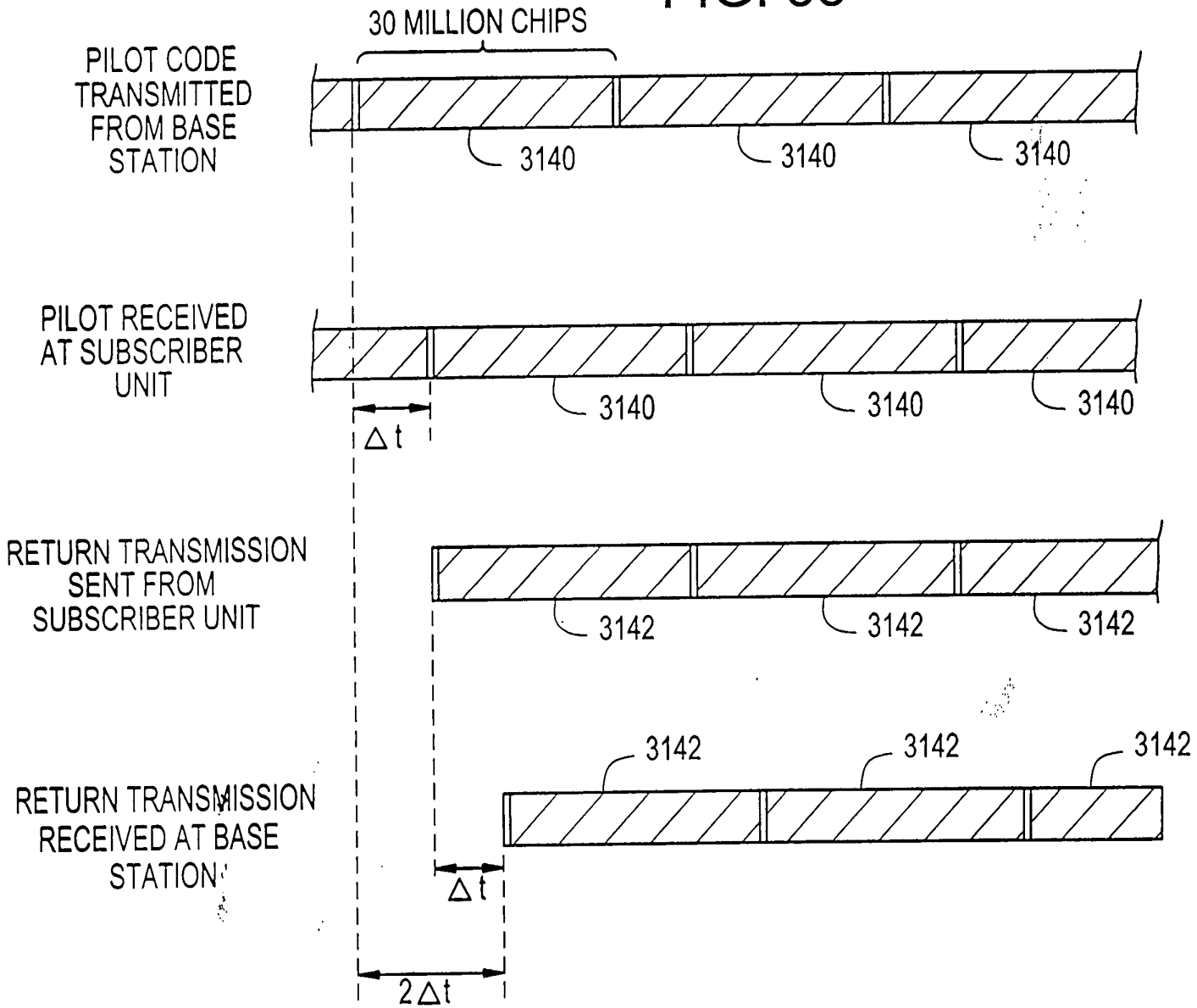

30 MILLION CHIPS
PILOT CODE TRANSMITTED FROM BASE STATION
3140
3140
3140
PILOT RECEIVED AT SUBSCRIBER UNIT
3140
3140
3140
Δt
RETURN TRANSMISSION SENT FROM SUBSCRIBER UNIT
3142
3142
3142
3142
3142
3142
RETURN TRANSMISSION RECEIVED AT BASE STATION
Δt
2Δt

FIG. 34

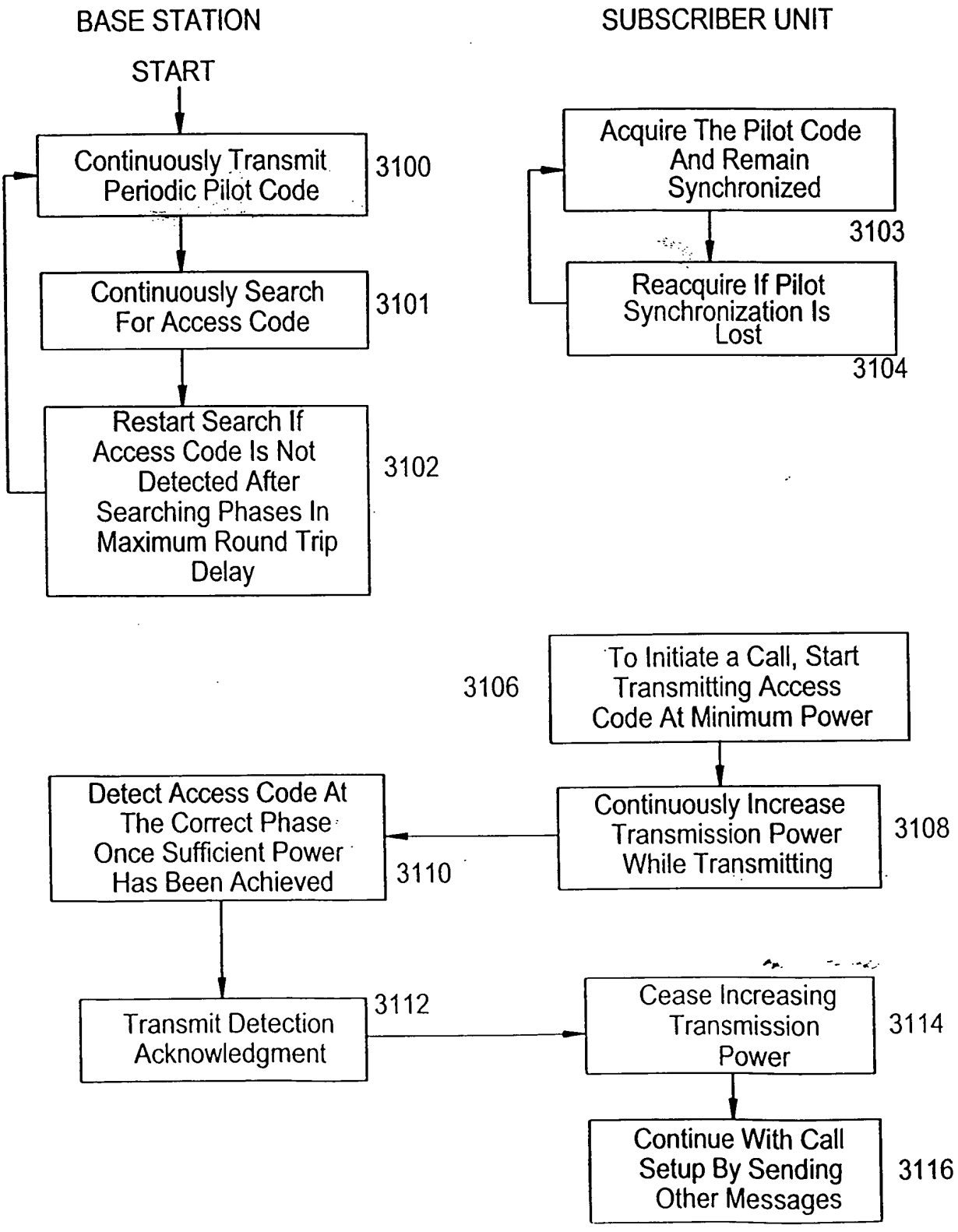

BASE STATION
SUBSCRIBER UNIT
START
Continuously Transmit Periodic Pilot Code
3100
Continuously Search For Access Code
3101
Restart Search If Access Code Is Not Detected After Searching Phases In Maximum Round Trip Delay
3102
Acquire The Pilot Code And Remain Synchronized
3103
Reacquire If Pilot Synchronization Is Lost
3104
3106
To Initiate a Call, Start Transmitting Access Code At Minimum Power
Continuously Increase Transmission Power While Transmitting
3108
Detect Access Code At The Correct Phase Once Sufficient Power Has Been Achieved
3110
Transmit Detection Acknowledgment
3112
Cease Increasing Transmission Power
3114
Continue With Call Setup By Sending Other Messages
3116

FIG. 35

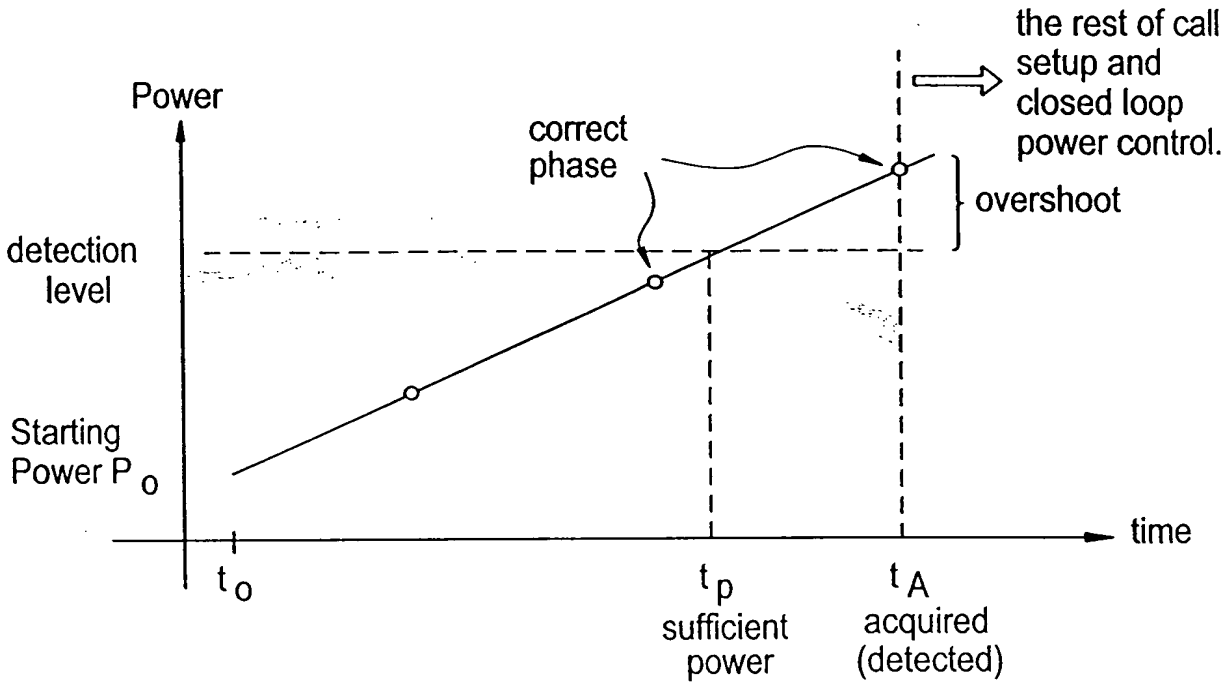

Power
correct phase
the rest of call setup and closed loop power control.
overshoot
detection level
Starting Power P o
time
t o
t p
sufficient power
t A
acquired (detected)

FIG. 37

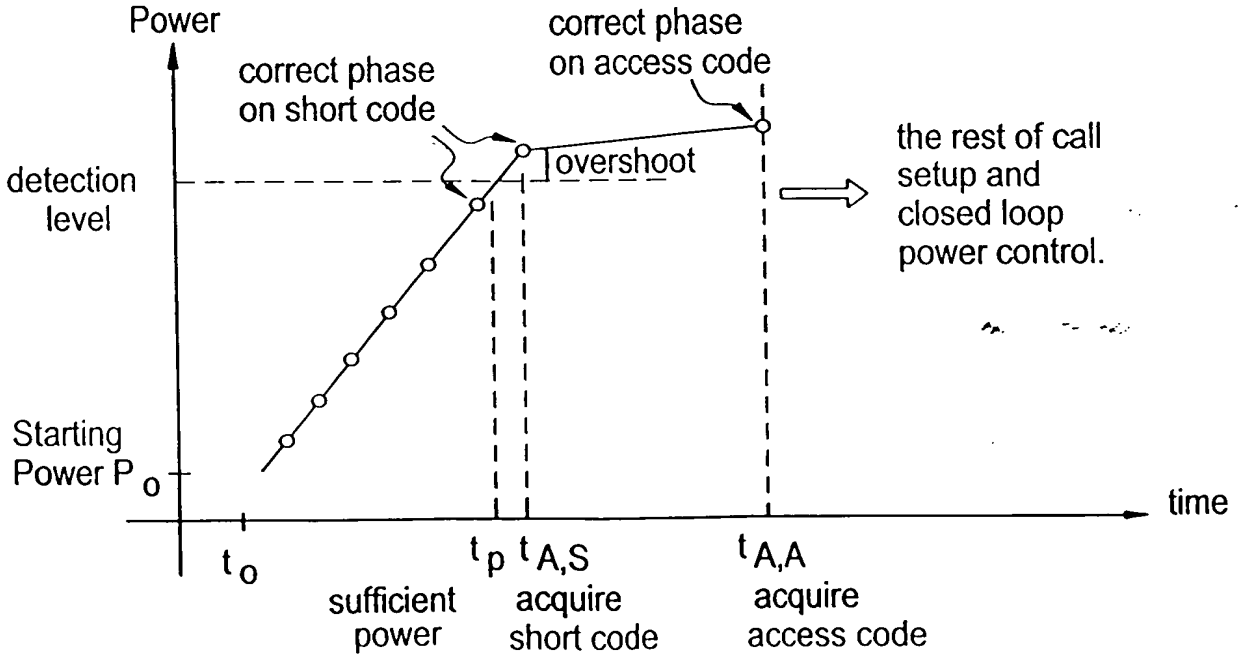

Power
correct phase on short code
correct phase on access code
overshoot
the rest of call setup and closed loop power control.
detection level
Starting Power P o
time
t o
t p
t A,S
t A,A
sufficient power
acquire short code
acquire access code

FIG. 36A

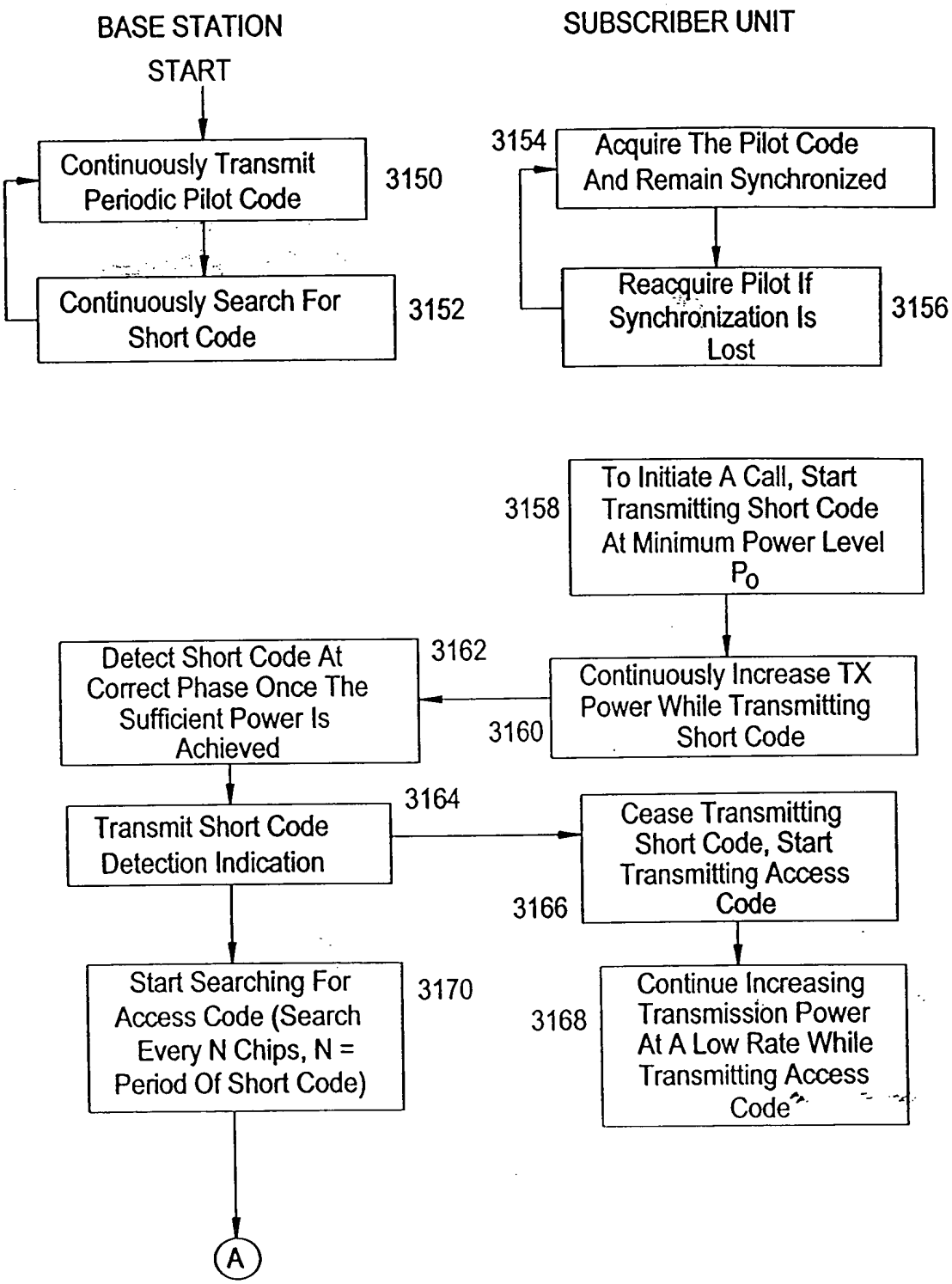

BASE STATION
SUBSCRIBER UNIT
START
Continuously Transmit Periodic Pilot Code
3150
Continuously Search For Short Code
3152
3154
Acquire The Pilot Code And Remain Synchronized
Reacquire Pilot If Synchronization Is Lost
3156
3158
To Initiate A Call, Start Transmitting Short Code At Minimum Power Level P_o
Continuously Increase TX Power While Transmitting Short Code
3160
Detect Short Code At Correct Phase Once The Sufficient Power Is Achieved
3162
Transmit Short Code Detection Indication
3164
Cease Transmitting Short Code, Start Transmitting Access Code
3166
Continue Increasing Transmission Power At A Low Rate While Transmitting Access Code
3168
Start Searching For Access Code (Search Every N Chips, N = Period Of Short Code)
3170
A

FIG. 36B

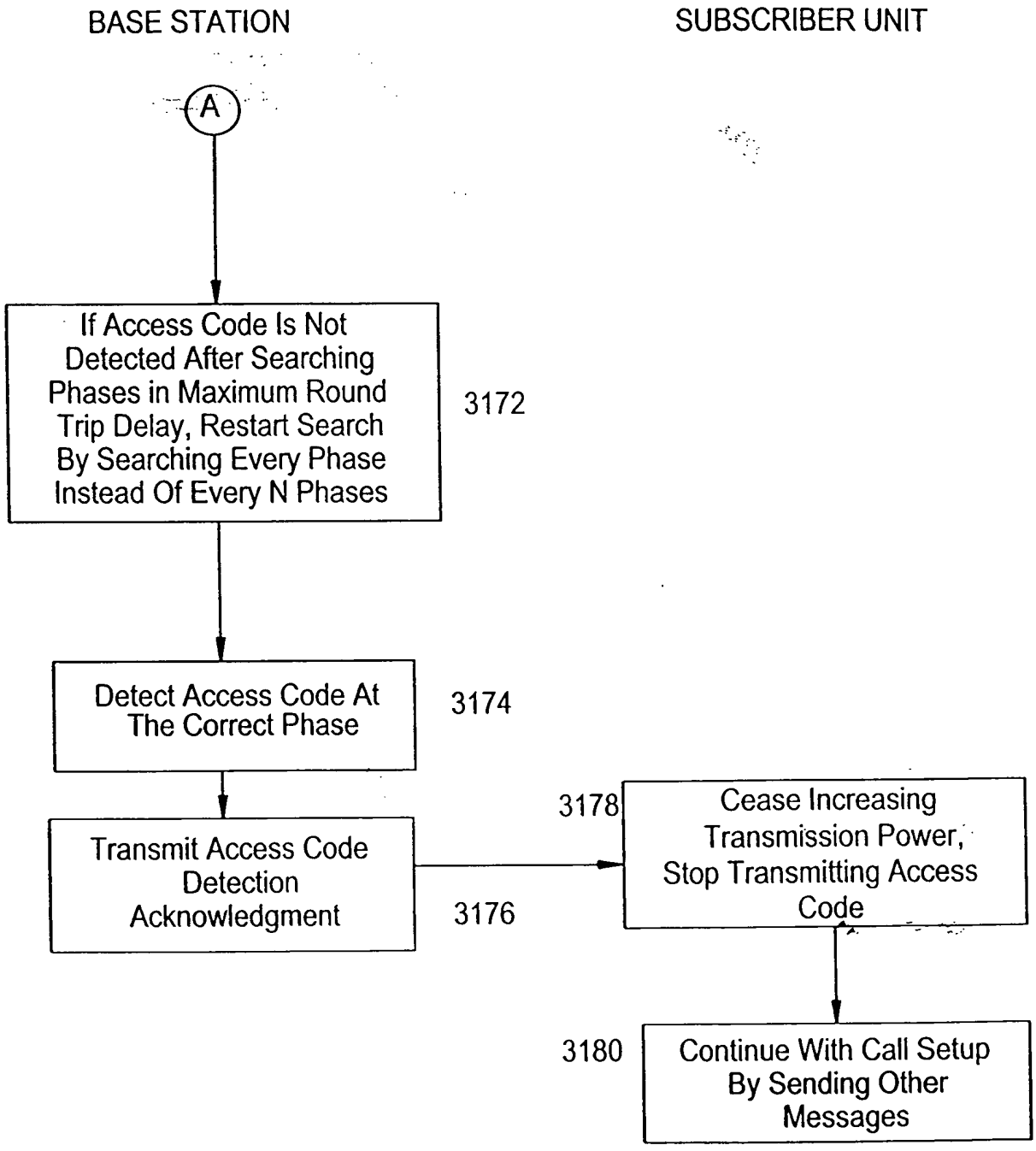

BASE STATION
SUBSCRIBER UNIT
A
If Access Code Is Not Detected After Searching Phases in Maximum Round Trip Delay, Restart Search By Searching Every Phase Instead Of Every N Phases
3172
Detect Access Code At The Correct Phase
3174
Transmit Access Code Detection Acknowledgment
3176
3178
Cease Increasing Transmission Power, Stop Transmitting Access Code
3180
Continue With Call Setup By Sending Other Messages

FIG. 38

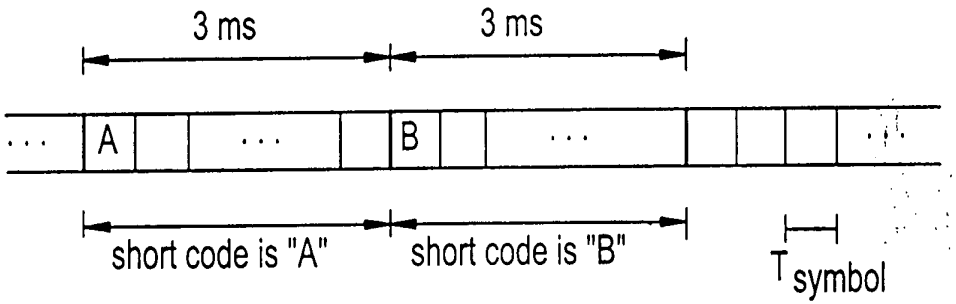

3 ms
3 ms
A
B
short code is "A"
short code is "B"
T symbol

FIG. 39

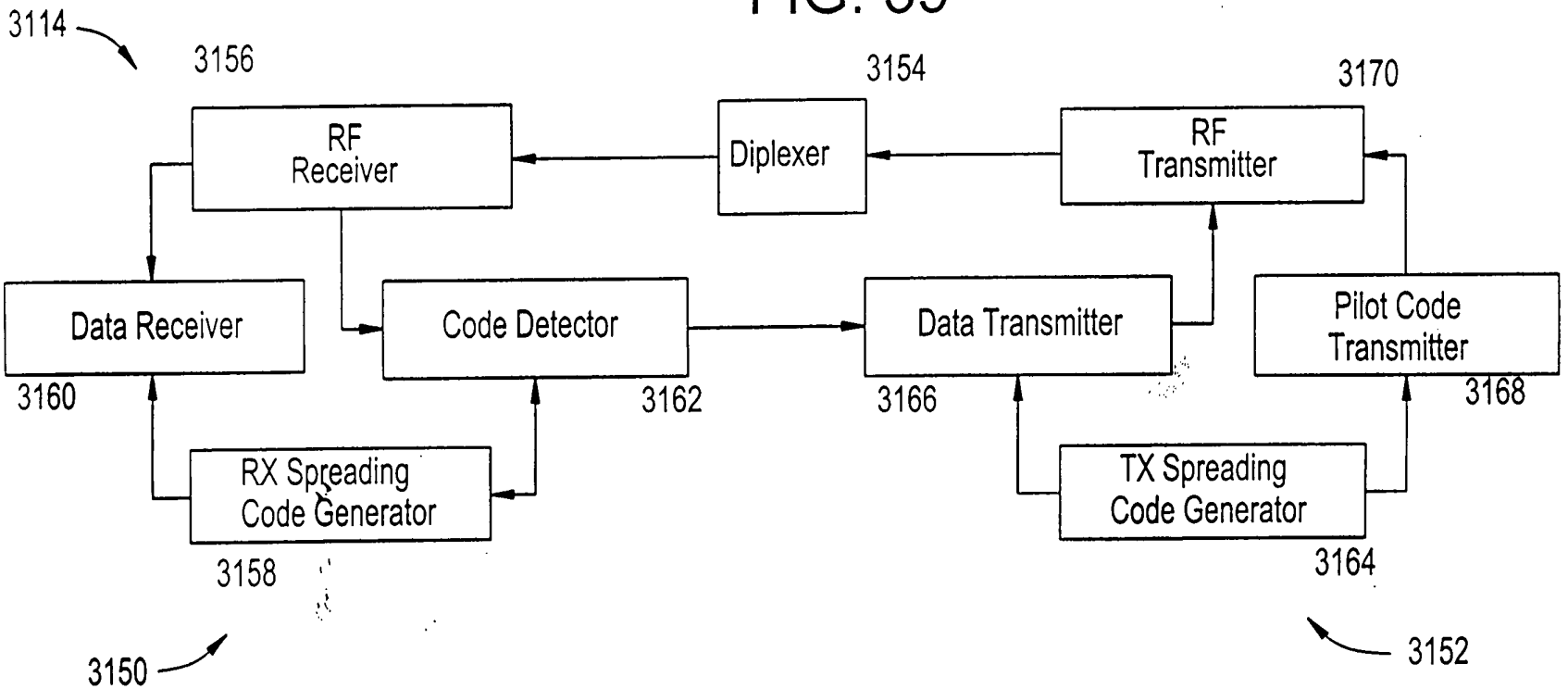

3114
3156
3154
3170
RF Receiver
Diplexer
RF Transmitter
Data Receiver
Code Detector
Data Transmitter
Pilot Code Transmitter
3160
3162
3166
3168
RX Spreading Code Generator
TX Spreading Code Generator
3158
3164
3150
3152

FIG. 40

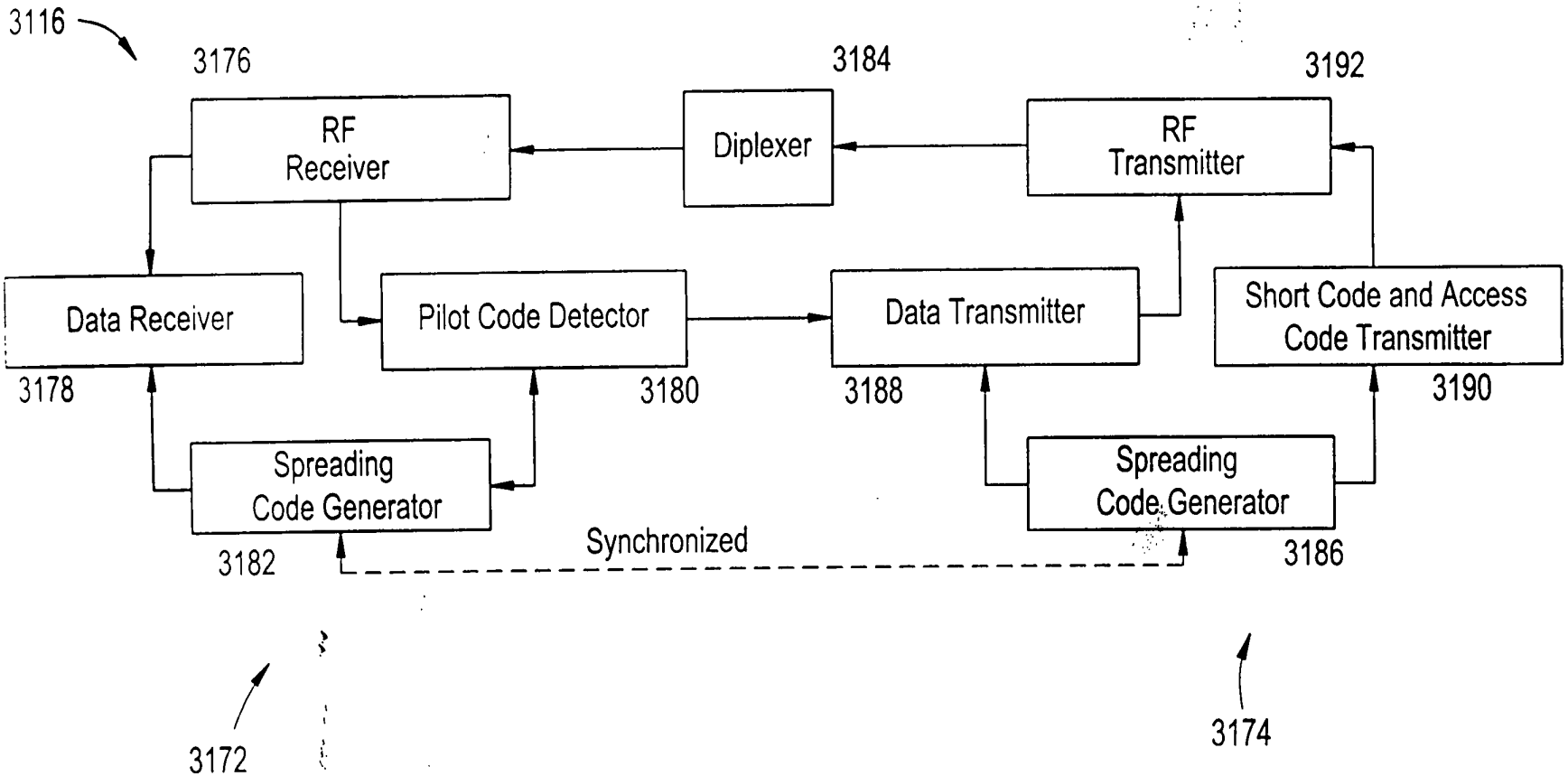

3116
3176
3184
3192
RF Receiver
Diplexer
RF Transmitter
Data Receiver
Pilot Code Detector
Data Transmitter
Short Code and Access Code Transmitter
3178
3180
3188
3190
Spreading Code Generator
Spreading Code Generator
Synchronized
3182
3186
3172
3174

FIG. 41A

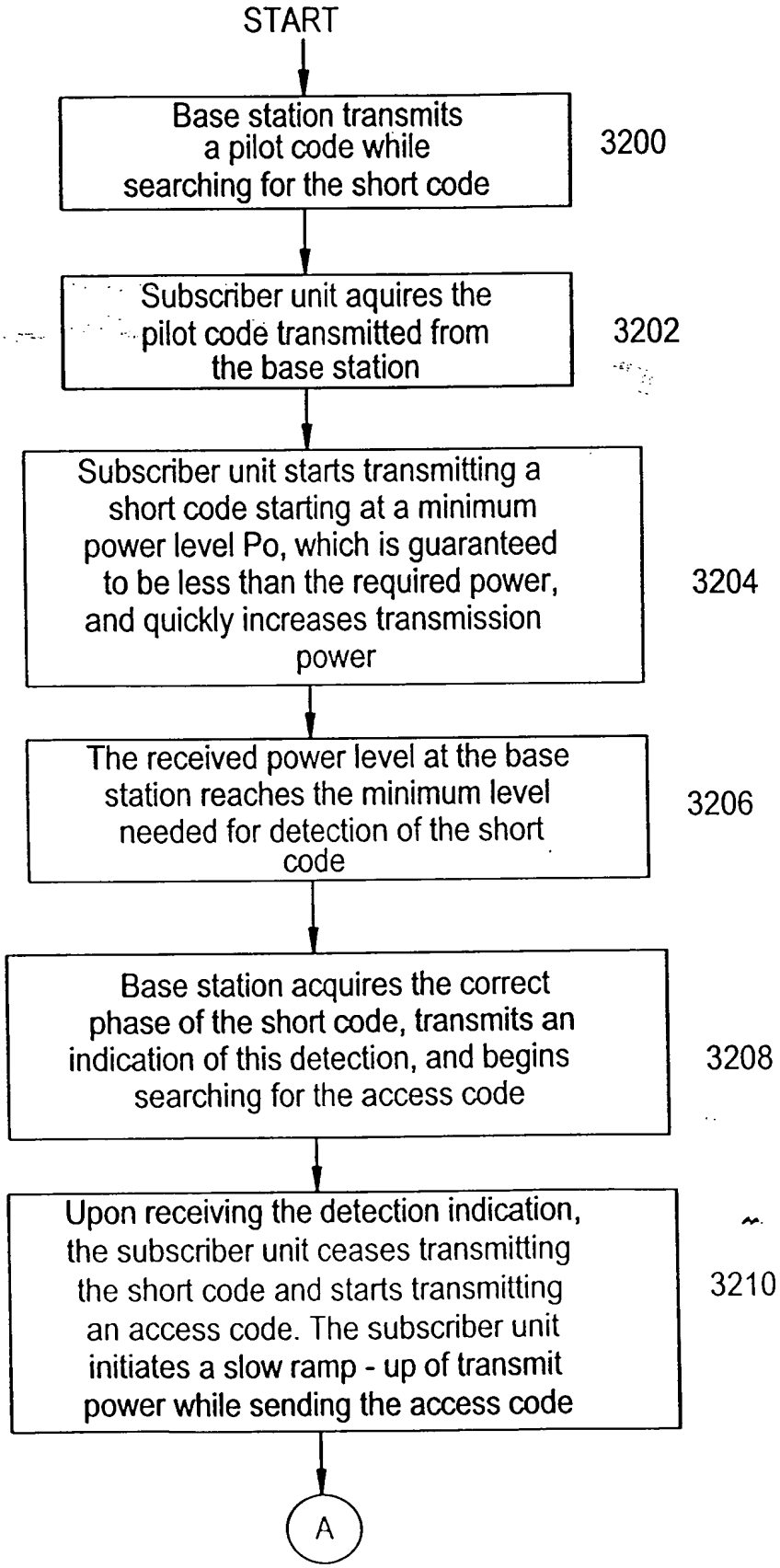

START
Base station transmits a pilot code while searching for the short code
3200
Subscriber unit aquires the pilot code transmitted from the base station
3202
Subscriber unit starts transmitting a short code starting at a minimum power level Po, which is guaranteed to be less than the required power, and quickly increases transmission power
3204
The received power level at the base station reaches the minimum level needed for detection of the short code
3206
Base station acquires the correct phase of the short code, transmits an indication of this detection, and begins searching for the access code
3208
Upon receiving the detection indication, the subscriber unit ceases transmitting the short code and starts transmitting an access code. The subscriber unit initiates a slow ramp - up of transmit power while sending the access code
3210
A

FIG. 41B

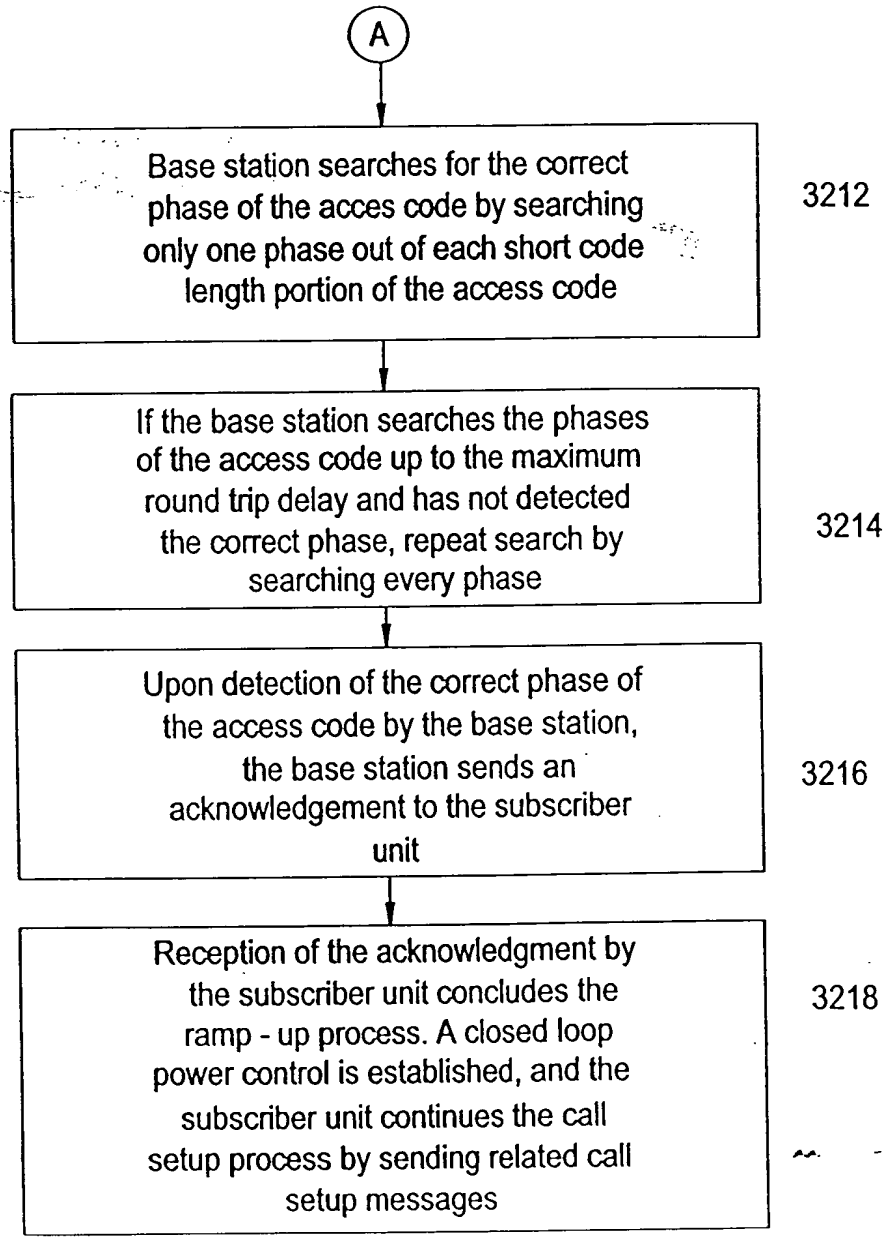

A
Base station searches for the correct phase of the acces code by searching only one phase out of each short code length portion of the access code
3212
If the base station searches the phases of the access code up to the maximum round trip delay and has not detected the correct phase, repeat search by searching every phase
3214
Upon detection of the correct phase of the access code by the base station, the base station sends an acknowledgement to the subscriber unit
3216
Reception of the acknowledgment by the subscriber unit concludes the ramp - up process. A closed loop power control is established, and the subscriber unit continues the call setup process by sending related call setup messages
3218

FIG. 42
PRIOR ART

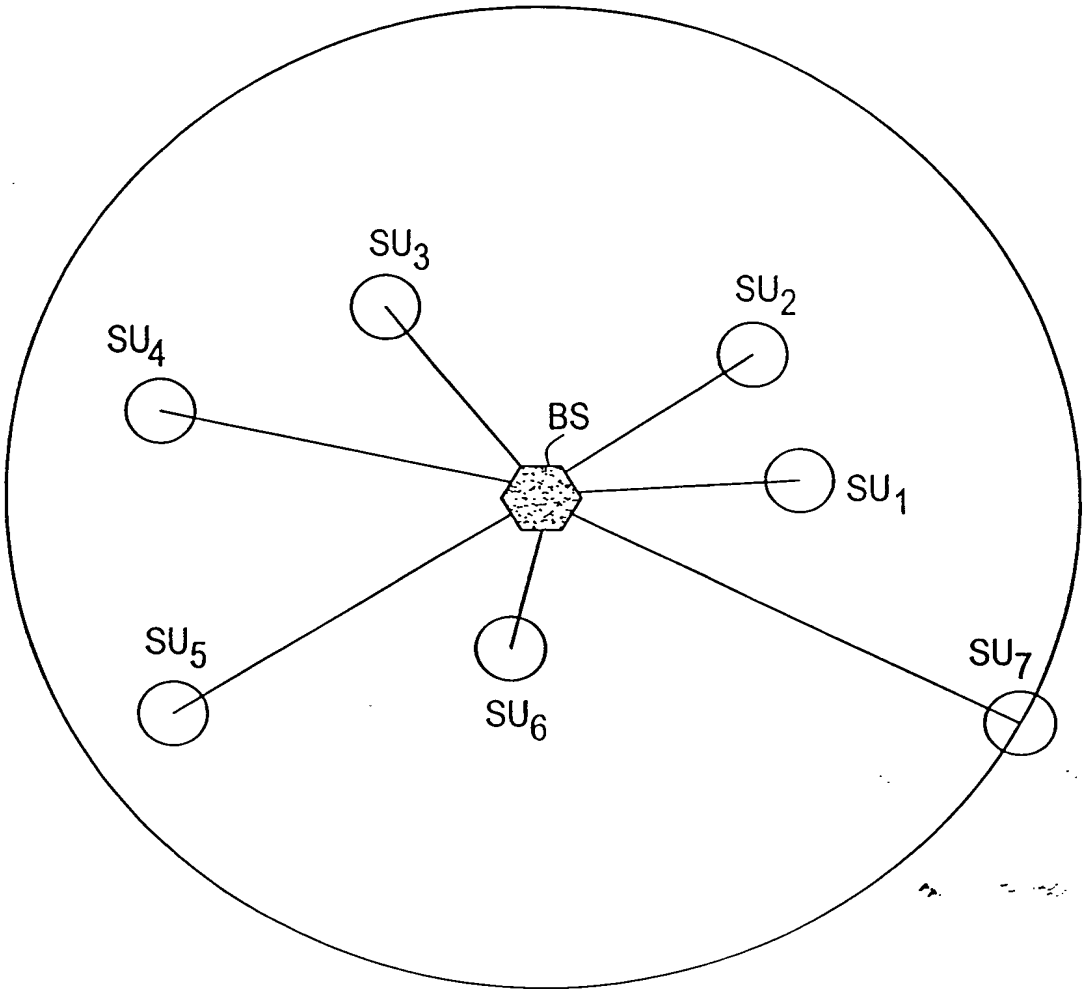


FIG. 43
(PRIOR ART)

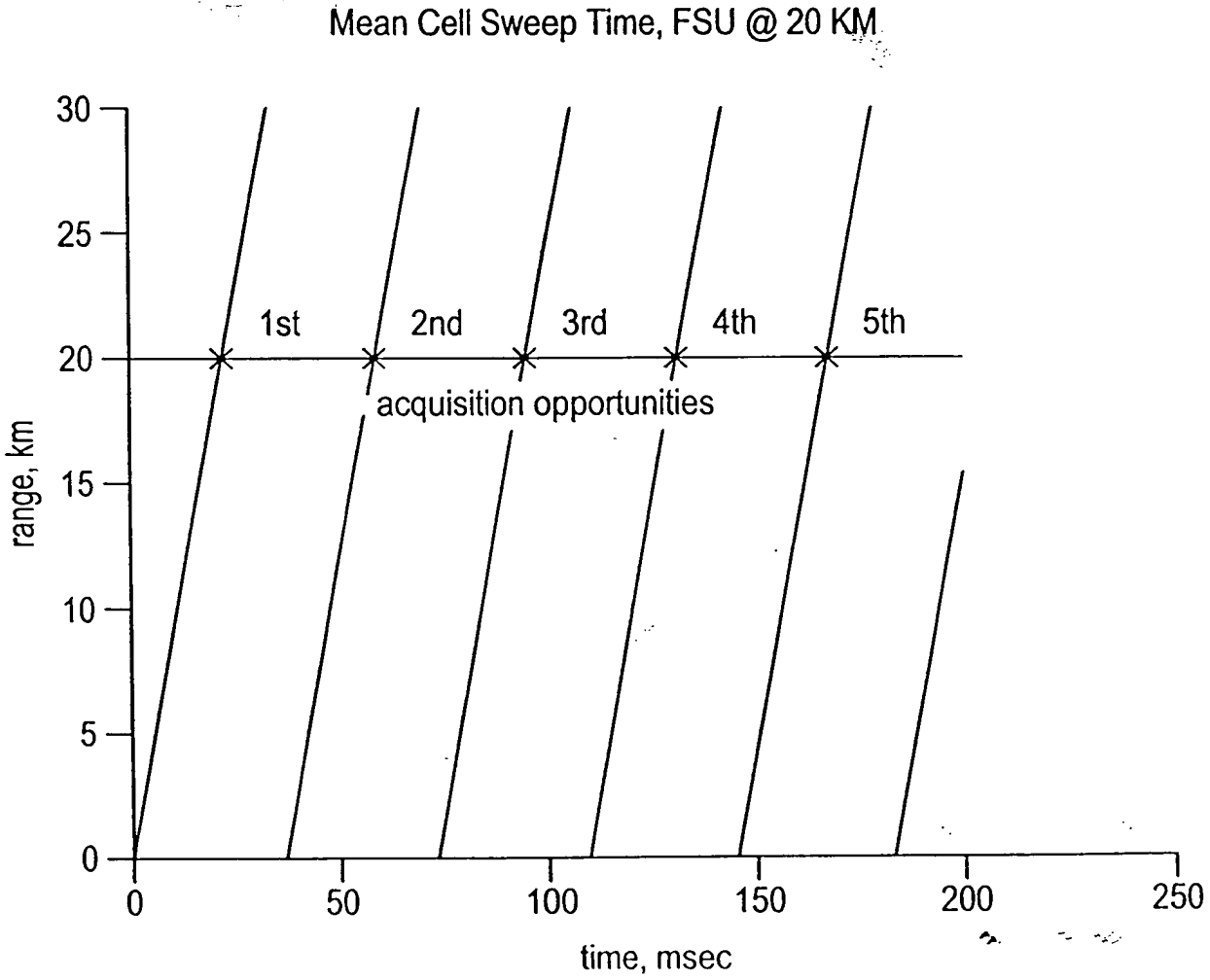


FIG.44

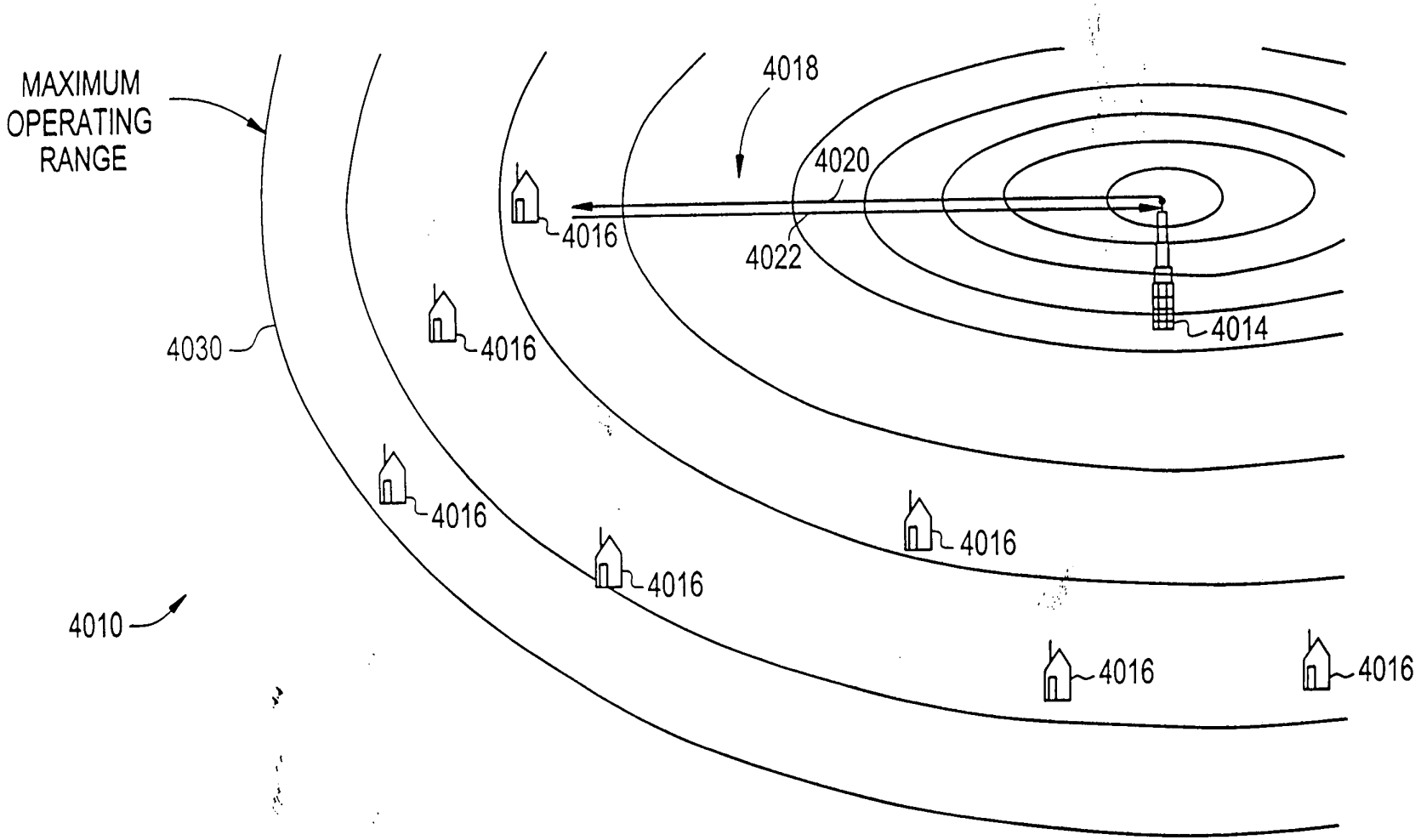

MAXIMUM
OPERATING
RANGE
4018
4020
4016
4022
4014
4030
4016
4016
4016
4016
4010
4016
4016

FIG. 45

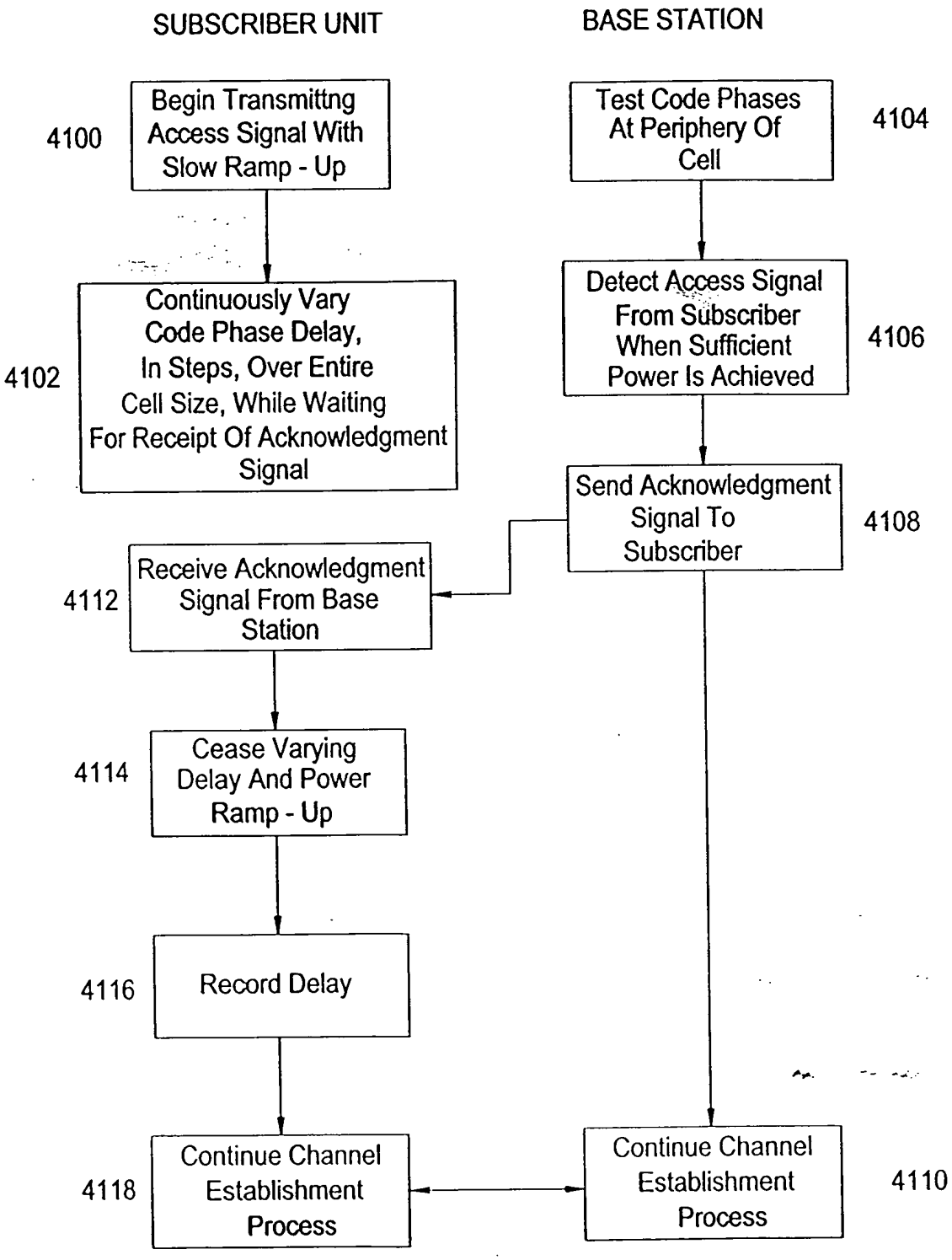

SUBSCRIBER UNIT
BASE STATION
4100
Begin Transmittng Access Signal With Slow Ramp - Up
4102
Continuously Vary Code Phase Delay, In Steps, Over Entire Cell Size, While Waiting For Receipt Of Acknowledgment Signal
4104
Test Code Phases At Periphery Of Cell
4106
Detect Access Signal From Subscriber When Sufficient Power Is Achieved
4108
Send Acknowledgment Signal To Subscriber
4112
Receive Acknowledgment Signal From Base Station
4114
Cease Varying Delay And Power Ramp - Up
4116
Record Delay
4118
Continue Channel Establishment Process
4110
Continue Channel Establishment Process

FIG. 46

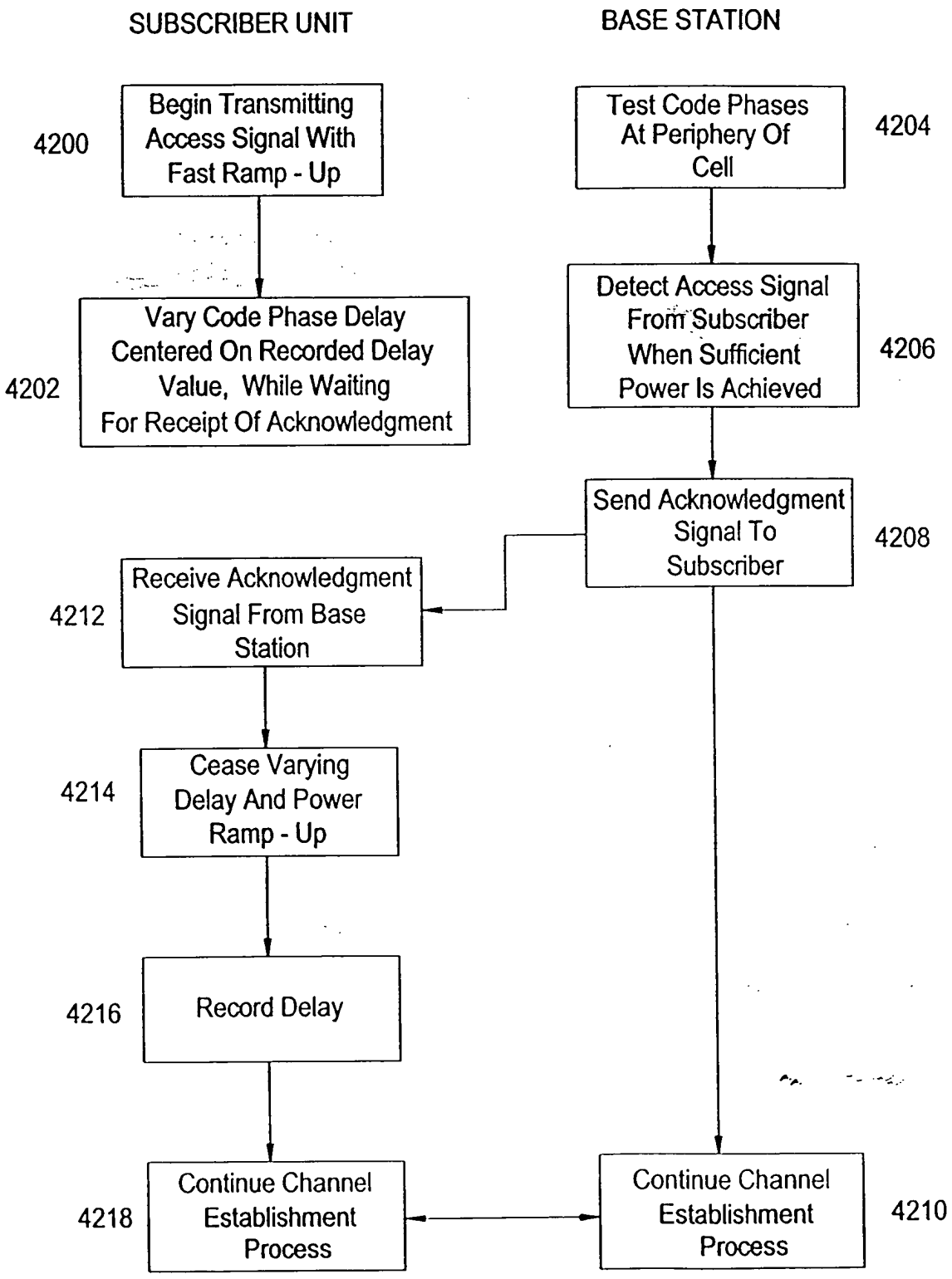

SUBSCRIBER UNIT
BASE STATION
4200
Begin Transmitting Access Signal With Fast Ramp - Up
4202
Vary Code Phase Delay Centered On Recorded Delay Value, While Waiting For Receipt Of Acknowledgment
4204
Test Code Phases At Periphery Of Cell
4206
Detect Access Signal From Subscriber When Sufficient Power Is Achieved
4208
Send Acknowledgment Signal To Subscriber
4212
Receive Acknowledgment Signal From Base Station
4214
Cease Varying Delay And Power Ramp - Up
4216
Record Delay
4218
Continue Channel Establishment Process
4210
Continue Channel Establishment Process

FIG. 47

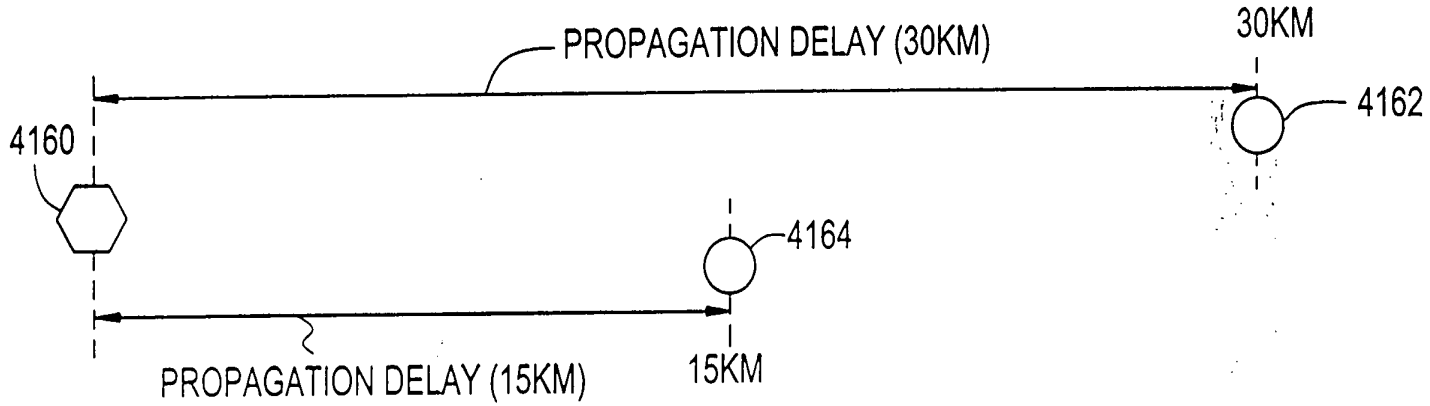

PROPAGATION DELAY (30KM)
30KM
4162
4160
4164
PROPAGATION DELAY (15KM)
15KM

FIG. 48

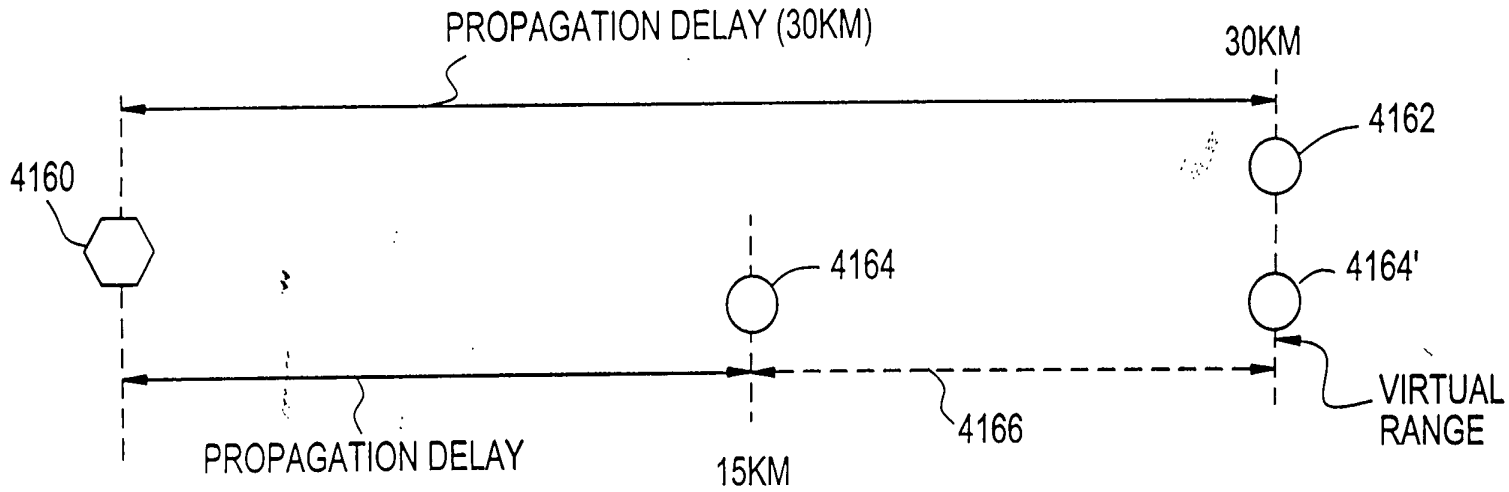

PROPAGATION DELAY (30KM)
30KM
4162
4160
4164
4164'
VIRTUAL
RANGE
4166
PROPAGATION DELAY
15KM

FIG. 49

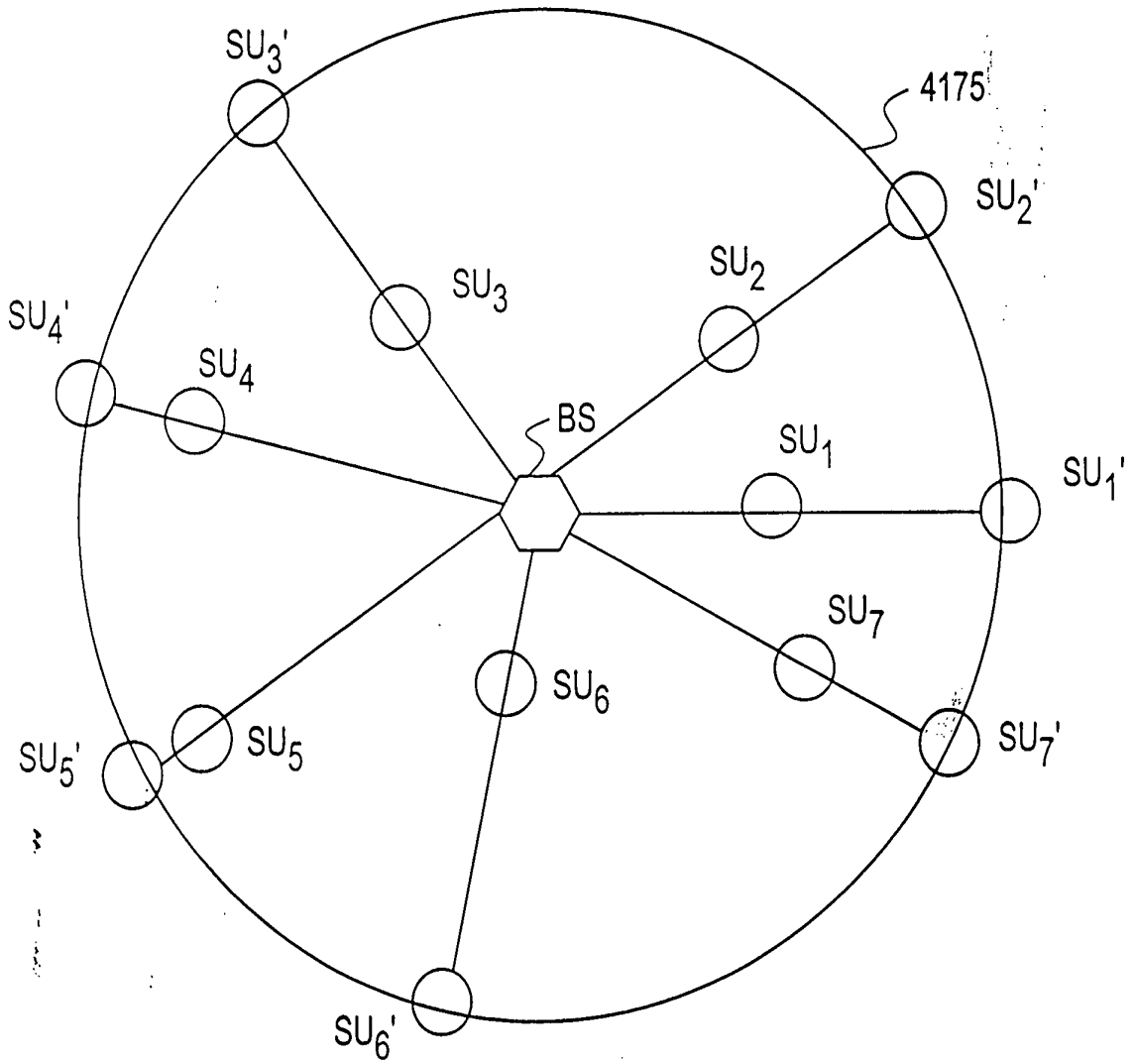


FIG. 50

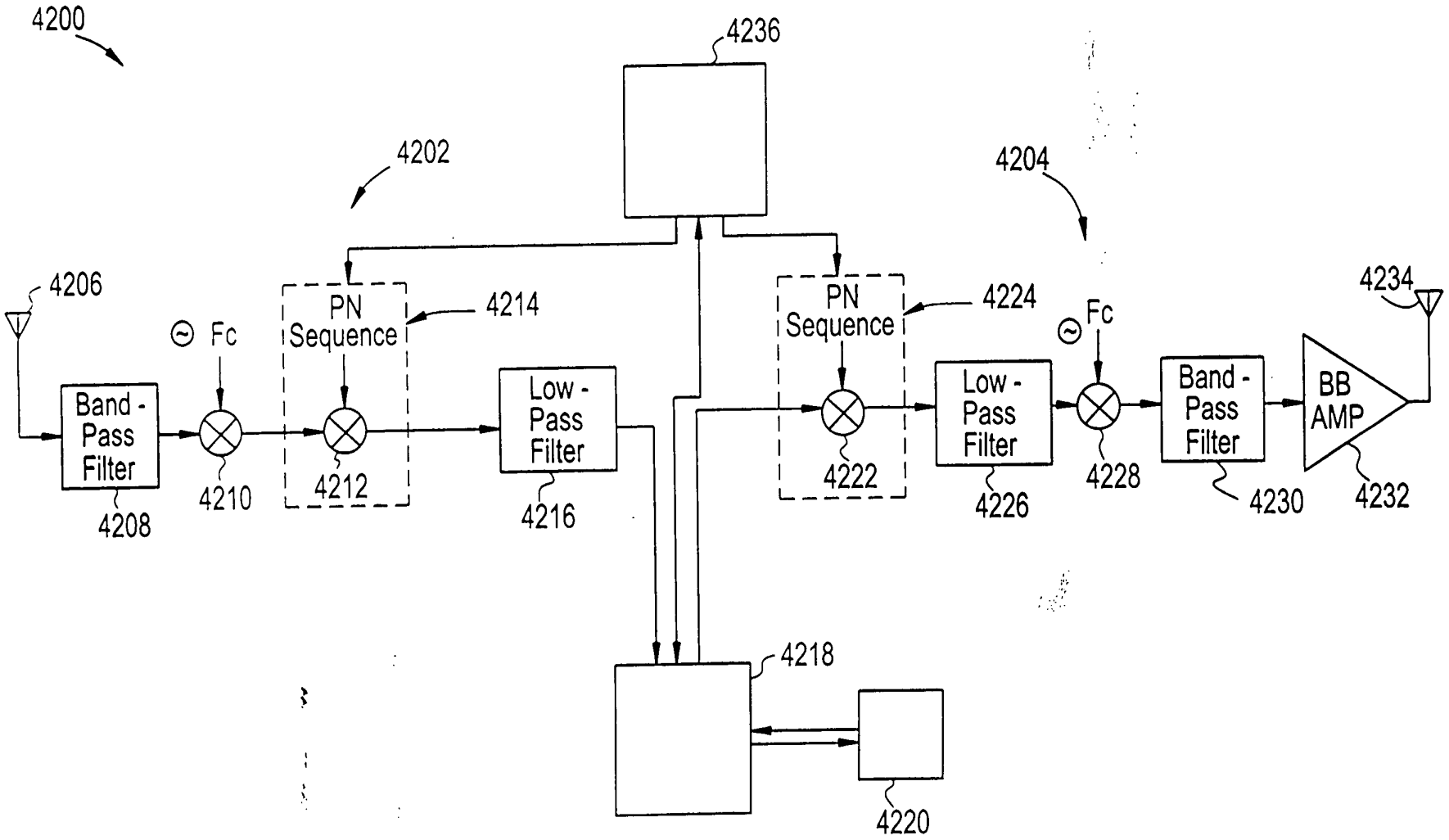

4200
4236
4202
4204
4206
Fc
PN Sequence
4214
PN Sequence
4224
Fc
4234
Band - Pass Filter
4208
4210
4212
Low - Pass Filter
4216
4222
Low - Pass Filter
4226
4228
Band - Pass Filter
4230
BB AMP
4232
4218
4220

FIG. 51

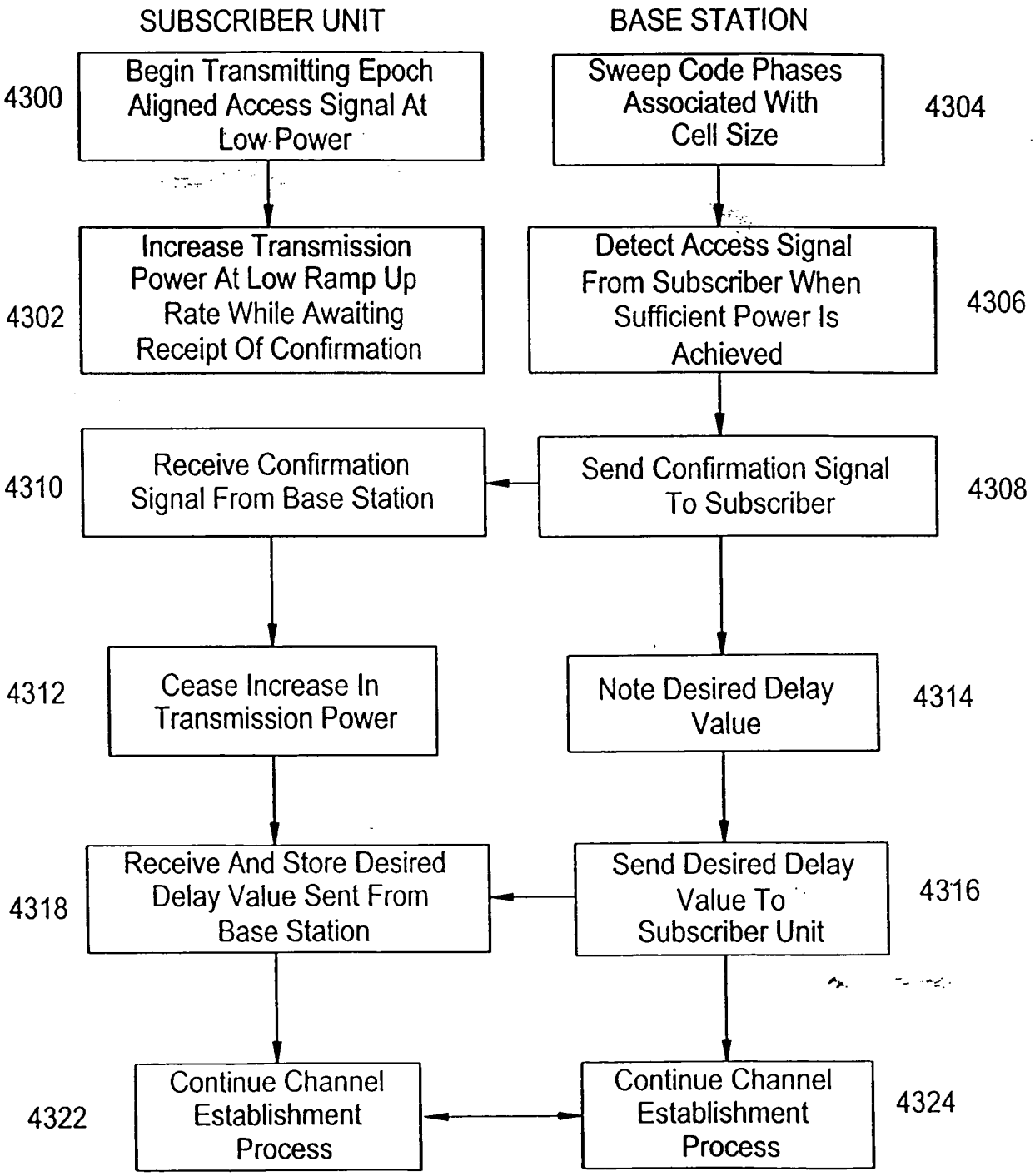

SUBSCRIBER UNIT
BASE STATION
4300
Begin Transmitting Epoch Aligned Access Signal At Low Power
Sweep Code Phases Associated With Cell Size
4304
4302
Increase Transmission Power At Low Ramp Up Rate While Awaiting Receipt Of Confirmation
Detect Access Signal From Subscriber When Sufficient Power Is Achieved
4306
4310
Receive Confirmation Signal From Base Station
Send Confirmation Signal To Subscriber
4308
4312
Cease Increase In Transmission Power
Note Desired Delay Value
4314
4318
Receive And Store Desired Delay Value Sent From Base Station
Send Desired Delay Value To Subscriber Unit
4316
4322
Continue Channel Establishment Process
Continue Channel Establishment Process
4324

FIG. 52

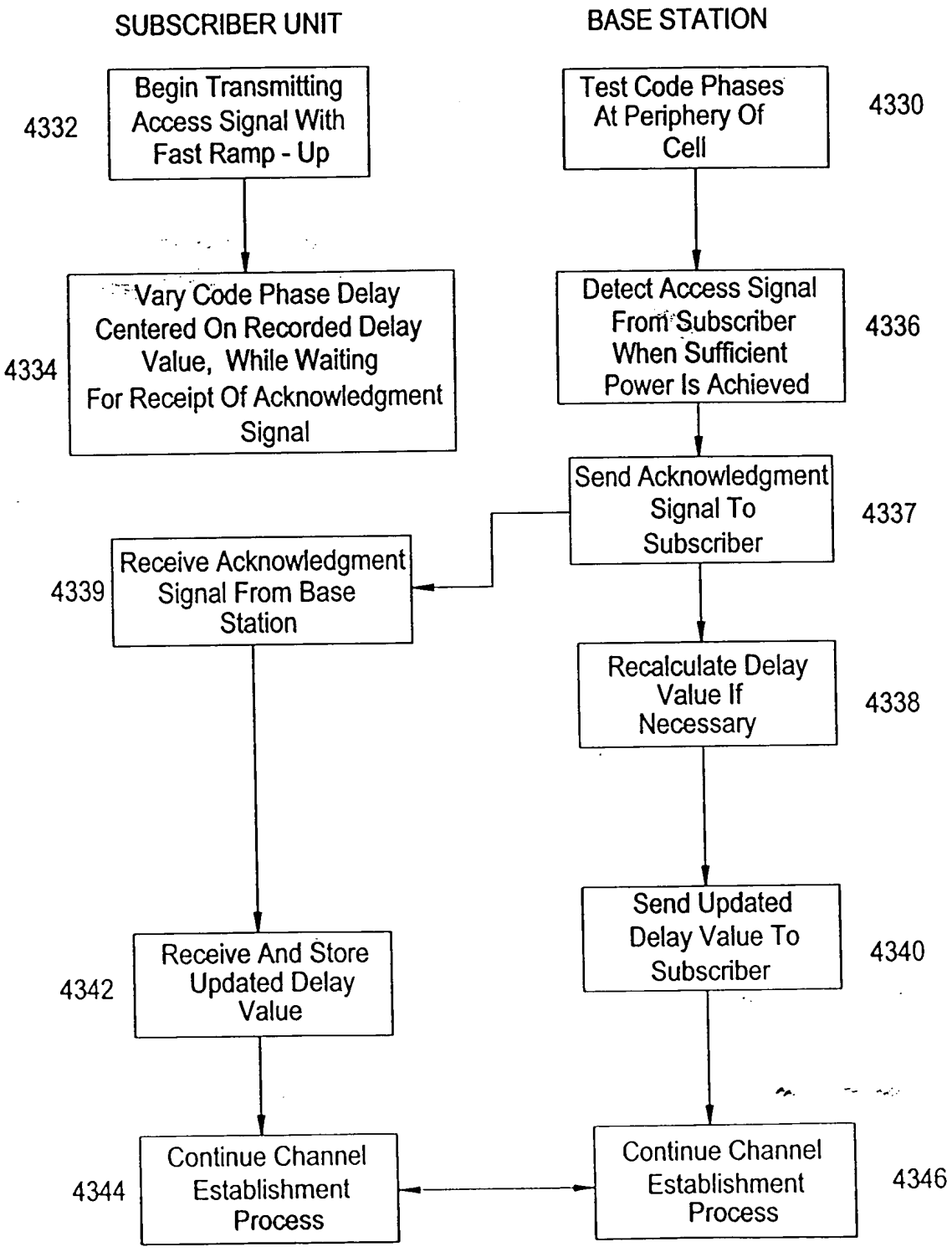

SUBSCRIBER UNIT
BASE STATION
Begin Transmitting Access Signal With Fast Ramp - Up
4332
Test Code Phases At Periphery Of Cell
4330
Vary Code Phase Delay Centered On Recorded Delay Value, While Waiting For Receipt Of Acknowledgment Signal
4334
Detect Access Signal From Subscriber When Sufficient Power Is Achieved
4336
Send Acknowledgment Signal To Subscriber
4337
Receive Acknowledgment Signal From Base Station
4339
Recalculate Delay Value If Necessary
4338
Send Updated Delay Value To Subscriber
4340
Receive And Store Updated Delay Value
4342
Continue Channel Establishment Process
4344
Continue Channel Establishment Process
4346

FIG. 53

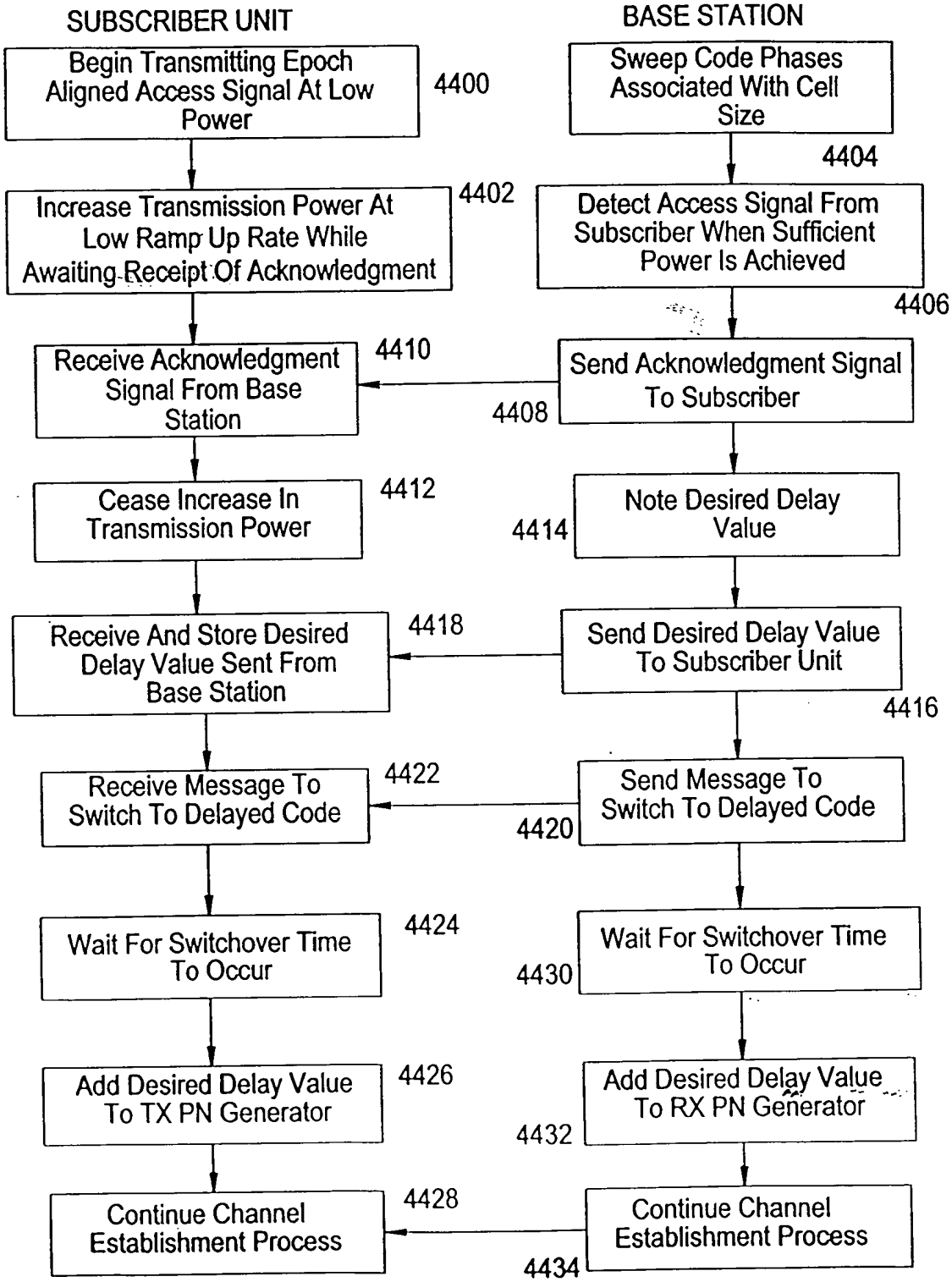

SUBSCRIBER UNIT
BASE STATION
Begin Transmitting Epoch Aligned Access Signal At Low Power
4400
Sweep Code Phases Associated With Cell Size
4404
Increase Transmission Power At Low Ramp Up Rate While Awaiting Receipt Of Acknowledgment
4402
Detect Access Signal From Subscriber When Sufficient Power Is Achieved
4406
Receive Acknowledgment Signal From Base Station
4410
Send Acknowledgment Signal To Subscriber
4408
Cease Increase In Transmission Power
4412
Note Desired Delay Value
4414
Receive And Store Desired Delay Value Sent From Base Station
4418
Send Desired Delay Value To Subscriber Unit
4416
Receive Message To Switch To Delayed Code
4422
Send Message To Switch To Delayed Code
4420
Wait For Switchover Time To Occur
4424
Wait For Switchover Time To Occur
4430
Add Desired Delay Value To TX PN Generator
4426
Add Desired Delay Value To RX PN Generator
4432
Continue Channel Establishment Process
4428
Continue Channel Establishment Process
4434

FIG. 54
PRIOR ART

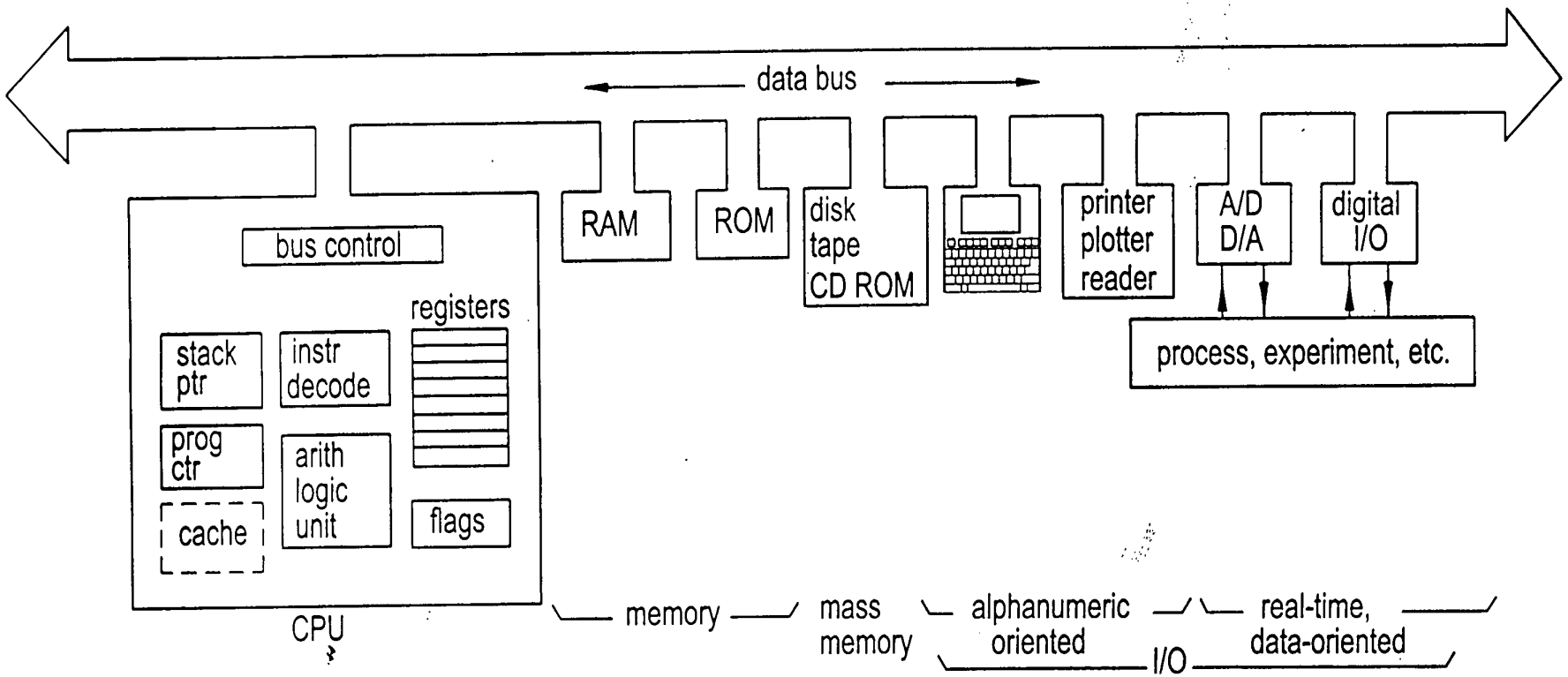


FIG. 55
PRIOR ART

BUS	RAW bandwidth (Mbyte/s)	Data width	Address width	Block xfer?	MUXed data/adr?	Multimaster?	Sync/Async	IRQ Lines a	Drivers	Connector b	Comments
STD bus		8	16	–	–	–	S	1	TTL	CE	controller-type applications
PC/XT	1.2	8	20	–	–	–	S	5E	TTL	CE	original IBM PC & compatibles
PC/AT	5.3	8,16	20,24	–	–	(c)	S	10E	TTL	CE	accepts PC/XT cards
EISA	33	8,16,32	20,24,32	•	–	•	S	11P	TTL	CE	enhanced PC/AT; auto-configure
MicroChannel	20	8,16,(32)	24,(32)	•	–	•	A	11	TTL	CE	IBM PS/2; auto-configure
Q - bus	2	16	22	•	•	•	A	4	(d)	CE	LSI-11,μVAX-I,II;daisy-chained IACK
Multibus I	10	8,16	20,24	–	–	•	A	8	TTL	CE	Intel; SUN-I and others
CAMAC	3	24	9	•	–	–	S	L	TTL/OC	CE	data acqusition & control bus
VAX BI	13.3	8,16,24,32	32	•	•	•	S	4	TTL	ZIF	VAX 780, 8600 series; parity
Multibus II	40	8,16,24,32	16,32	•	•	•	S	M	TTL	DIN	parity; 40MB/s for blk xfer, 20M otherwise
NuBus	40	32	32	•	•	•	S	M	TTL	DIN	Macintosh II adds 1 dedicated INT per slot; ""
VME	40	8,16,32	16,24,32	•	–	•	A	7	TTL	DIN	daisy-chained IACK; SUN-3
Futurebus	120					•	A	–	(d)		
Fastbus	160	32	32	•	•	•	A	M	ECL	H	communication across many crates

(a) E-edge-sensitive;L-LAM ("look at me");M-"int" via bus mastership;
P-programmable edge-or-level-sensitive interrupts.

(b) CE-card-edge; DIN-2-part "Eurocard" 96-pin connector;
H-high density 2-part conn. (c) almost. (d) National Semi special.

FIG. 56

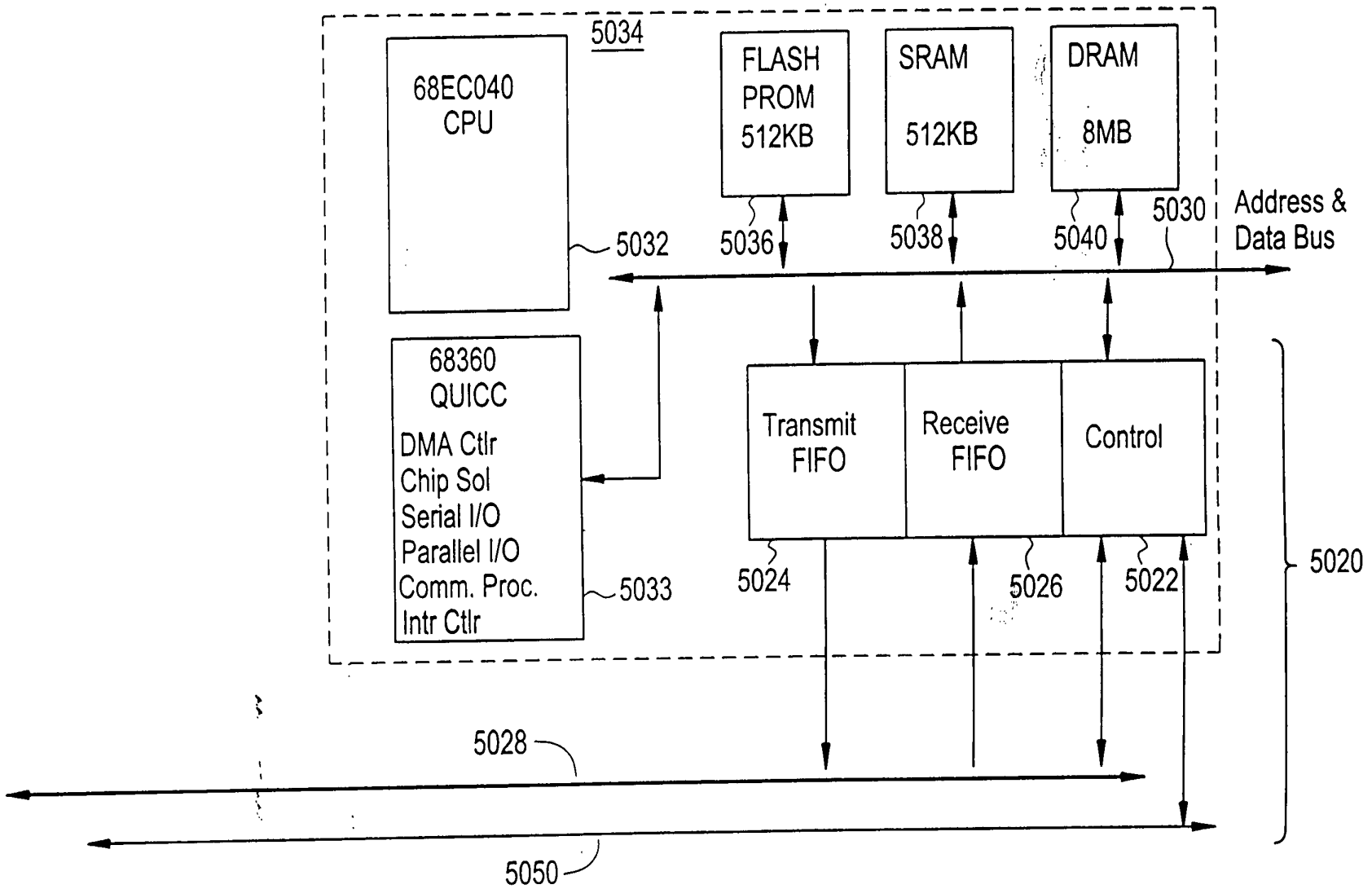
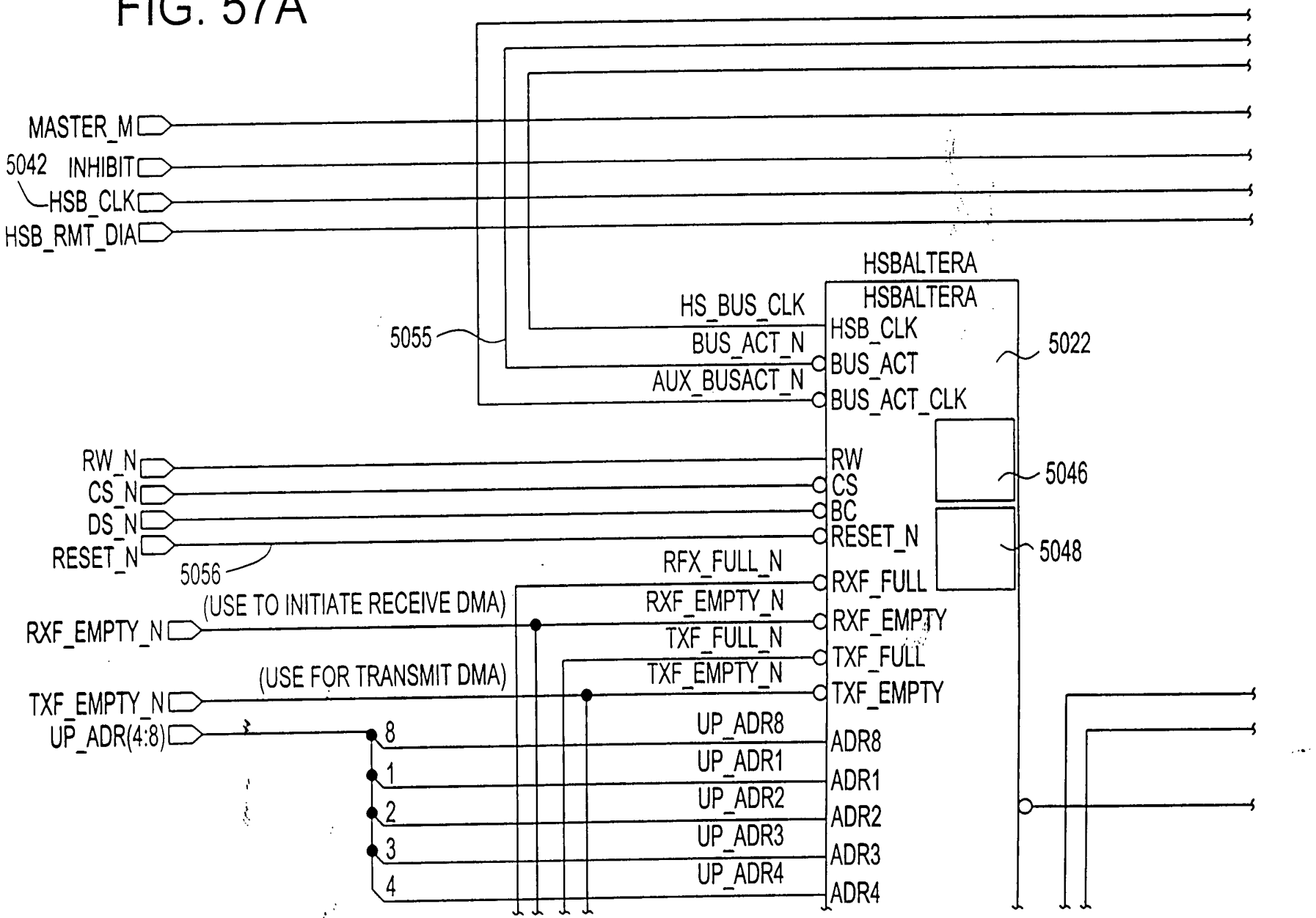

5034
68EC040
CPU
FLASH
PROM
512KB
SRAM
512KB
DRAM
8MB
5032
5036
5038
5040
5030
Address &
Data Bus
68360
QUICC
DMA Ctlr
Chip Sol
Serial I/O
Parallel I/O
Comm. Proc.
Intr Ctlr
5033
Transmit
FIFO
Receive
FIFO
Control
5024
5026
5022
5020
5028
5050

FIG. 57A


MASTER_M
5042
INHIBIT
HSB_CLK
HSB_RMT_DIA
HSBALTERA
HSBALTERA
HS_BUS_CLK
HSB_CLK
5055
BUS_ACT_N
BUS_ACT
5022
AUX_BUSACT_N
BUS_ACT_CLK
RW_N
CS_N
DS_N
RESET_N
5056
RW
CS
BC
RESET_N
5046
5048
RFX_FULL_N
RXF_FULL
(USE TO INITIATE RECEIVE DMA)
RXF_EMPTY_N
RXF_EMPTY_N
RXF_EMPTY
TXF_FULL_N
TXF_FULL
(USE FOR TRANSMIT DMA)
TXF_EMPTY_N
TXF_EMPTY_N
TXF_EMPTY
UP_ADR(4:8)
8
1
2
3
4
UP_ADR8
UP_ADR1
UP_ADR2
UP_ADR3
UP_ADR4
ADR8
ADR1
ADR2
ADR3
ADR4

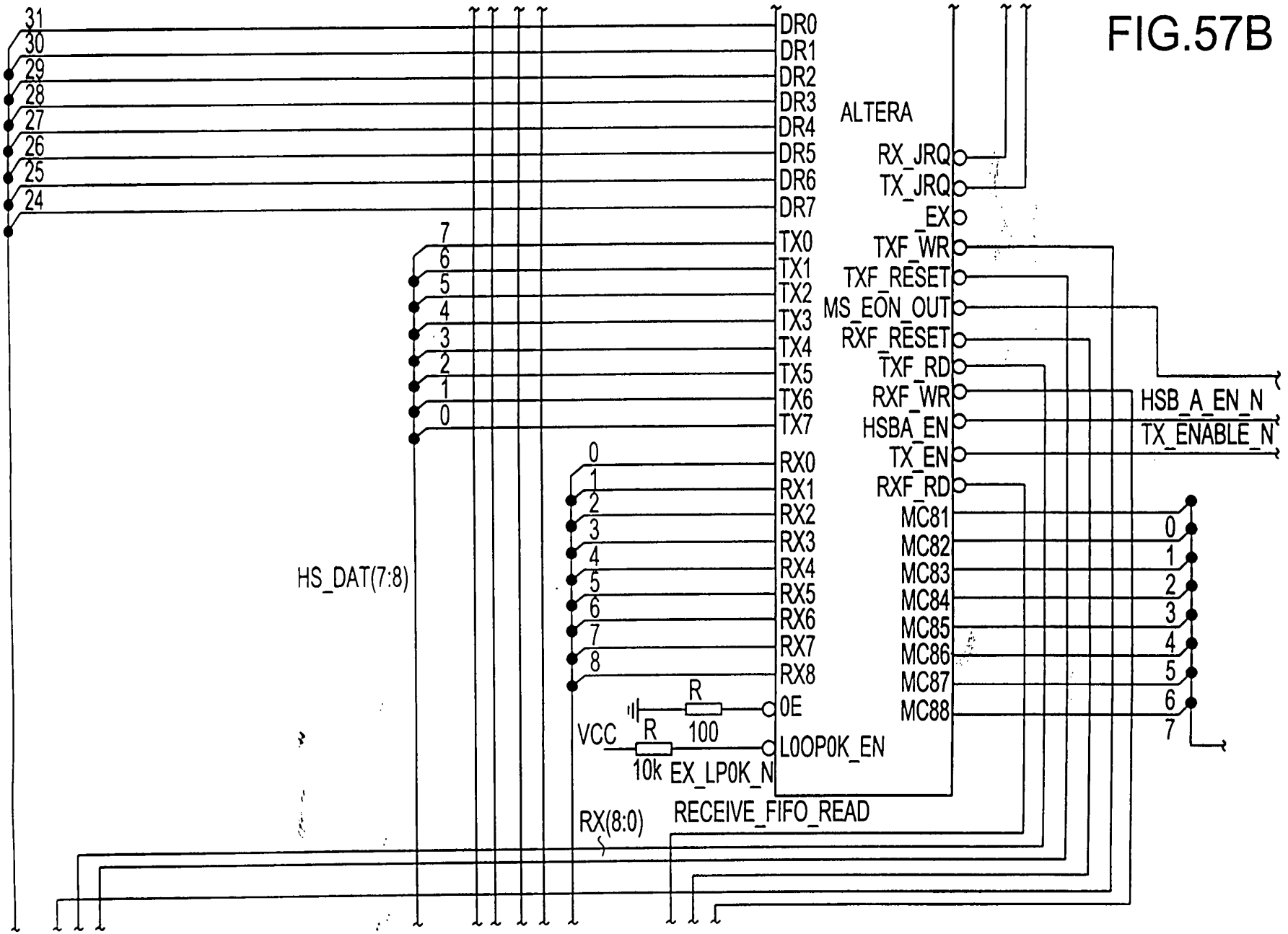

31
30
29
28
27
26
25
24
7
6
5
4
3
2
1
0
HS_DAT(7:8)
DR0
DR1
DR2
DR3
DR4
DR5
DR6
DR7
TX0
TX1
TX2
TX3
TX4
TX5
TX6
TX7
0
1
2
3
4
5
6
7
8
RX0
RX1
RX2
RX3
RX4
RX5
RX6
RX7
RX8
R
0E
VCC
R
100
L0OP0K_EN
10k
EX_LP0K_N
RX(8:0)
RECEIVE_FIFO_READ
ALTERA
RX_JRQ
TX_JRQ
_EX
TXF_WR
TXF_RESET
MS_EON_OUT
RXF_RESET
TXF_RD
RXF_WR
HSBA_EN
TX_EN
RXF_RD
MC81
MC82
MC83
MC84
MC85
MC86
MC87
MC88
HSB_A_EN_N
TX_ENABLE_N
0
1
2
3
4
5
6
7

FIG.57B

FIG. 57C

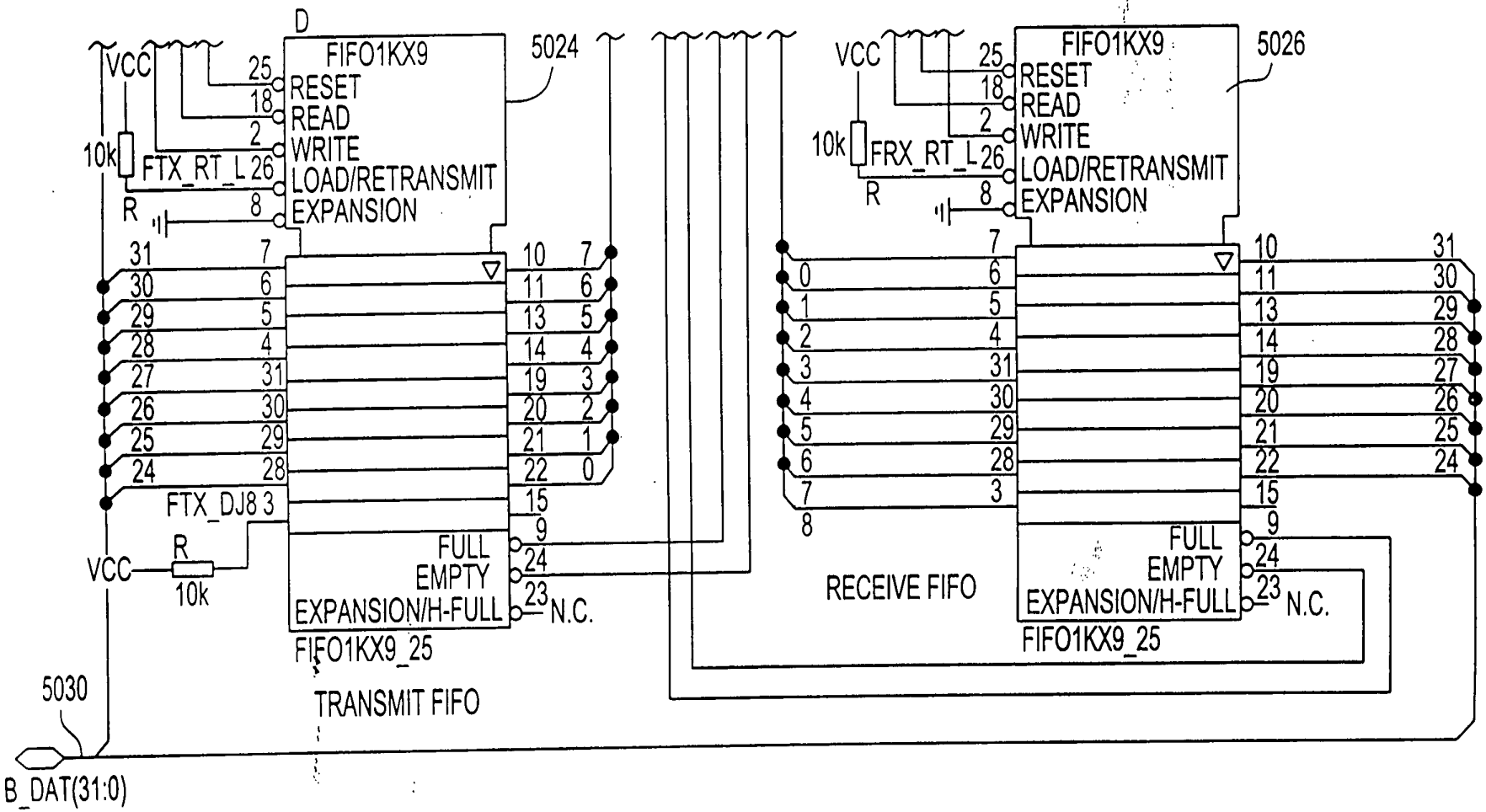

D
FIFO1KX9
5024
VCC
10k
FTX_RT_L
R
RESET
READ
WRITE
LOAD/RETRANSMIT
EXPANSION
FTX_DJ8
FULL
EMPTY
EXPANSION/H-FULL
N.C.
FIFO1KX9_25
TRANSMIT FIFO
FIFO1KX9
5026
FRX_RT_L
RECEIVE FIFO
5030
B_DAT(31:0)

FIG. 57D

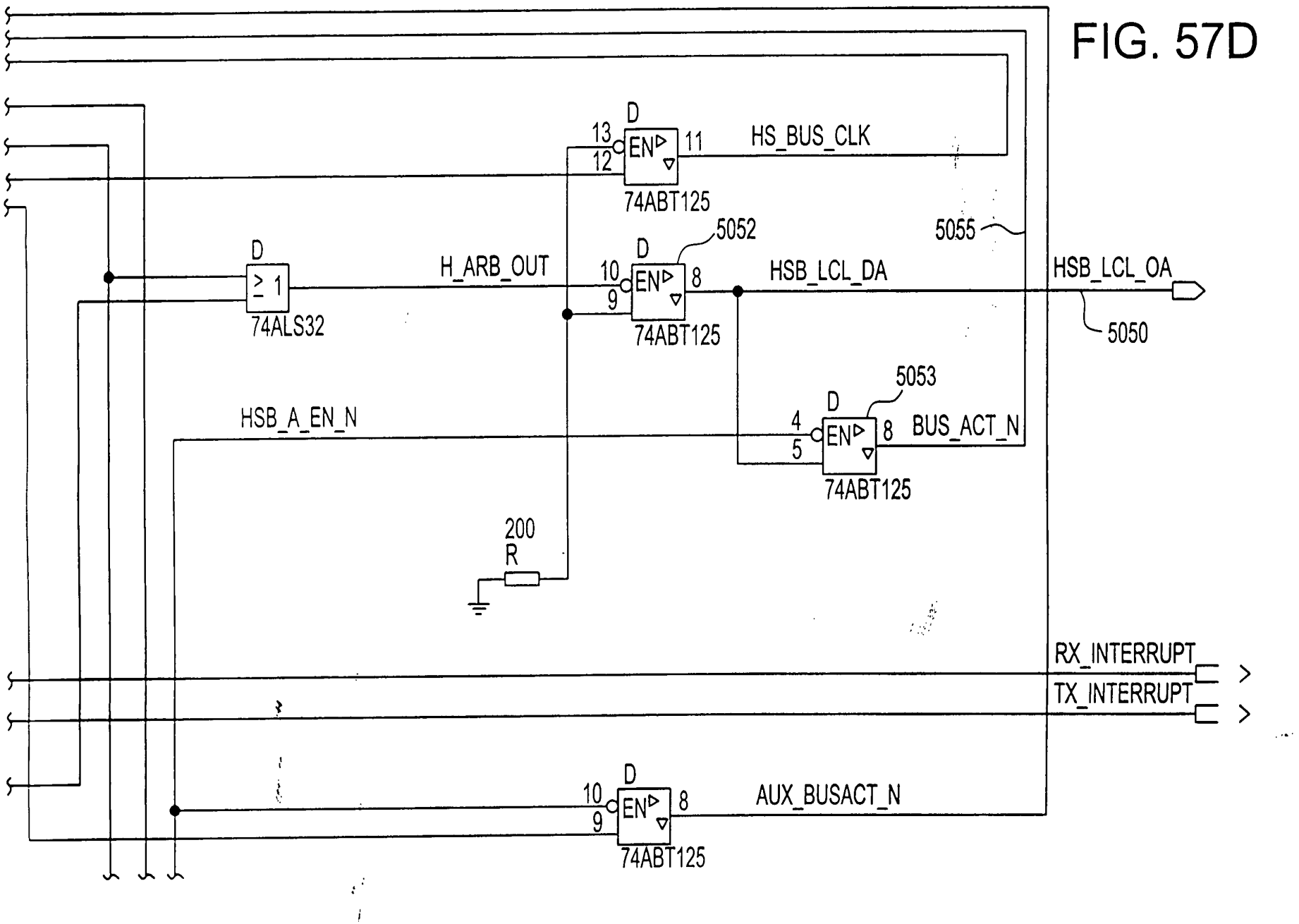

D
13
12
EN
11
HS_BUS_CLK
74ABT125
5052
5055
D
≥ 1
H_ARB_OUT
10
9
EN
8
HSB_LCL_DA
HSB_LCL_OA
74ALS32
74ABT125
5050
5053
D
HSB_A_EN_N
4
5
EN
8
BUS_ACT_N
74ABT125
200
R
RX_INTERRUPT
TX_INTERRUPT
D
10
9
EN
8
AUX_BUSACT_N
74ABT125

FIG. 57E

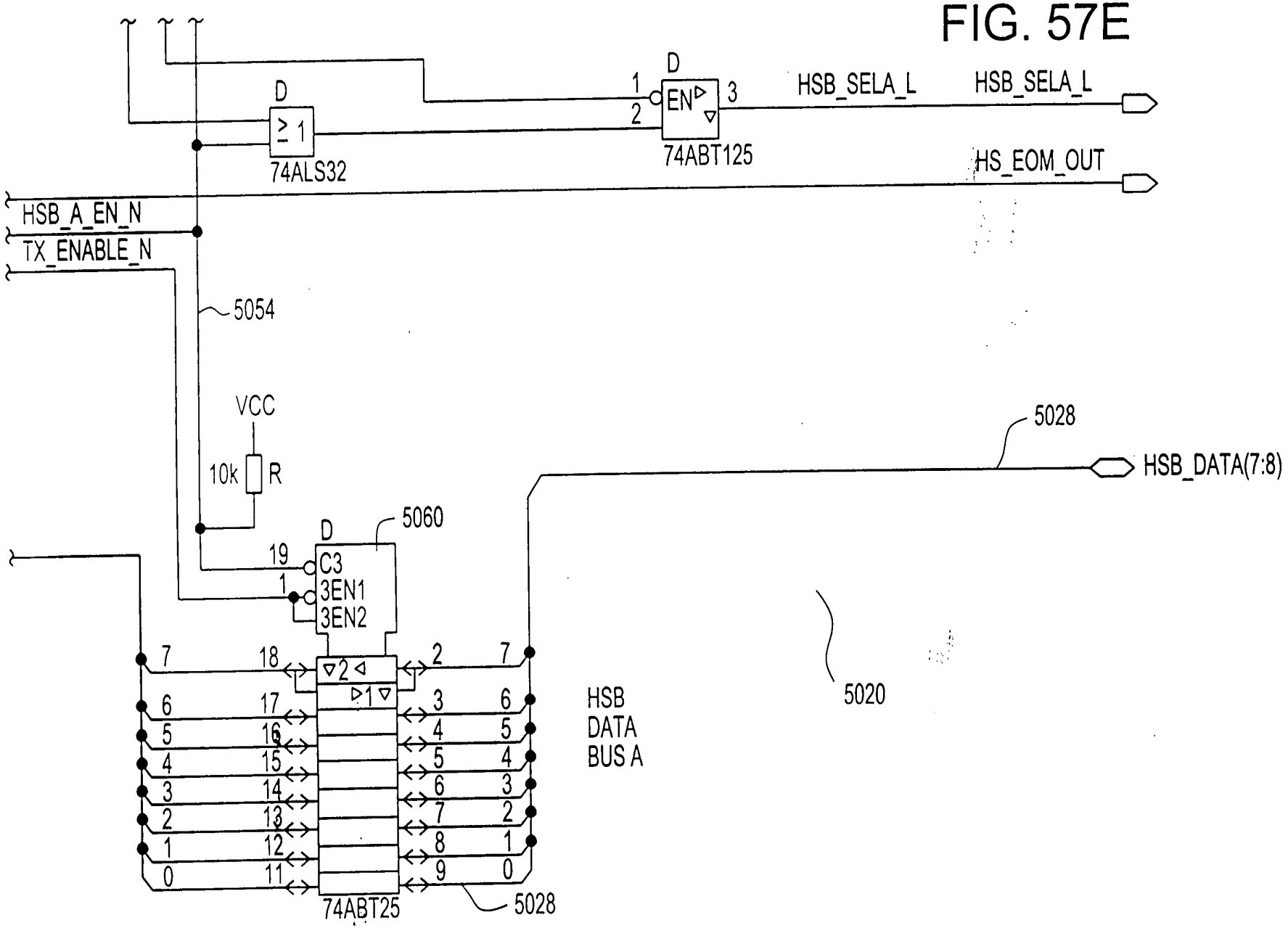

D
≥ 1
74ALS32
D
1
2
EN
3
74ABT125
HSB_SELA_L
HSB_SELA_L
HS_EOM_OUT
HSB_A_EN_N
TX_ENABLE_N
5054
VCC
10k
R
5028
HSB_DATA(7:8)
5060
D
19
C3
1
3EN1
3EN2
7
18
2
7
6
17
3
6
5
16
4
5
4
15
5
4
3
14
6
3
2
13
7
2
1
12
8
1
0
11
9
0
74ABT25
5028
HSB
DATA
BUS A
5020

FIG. 58

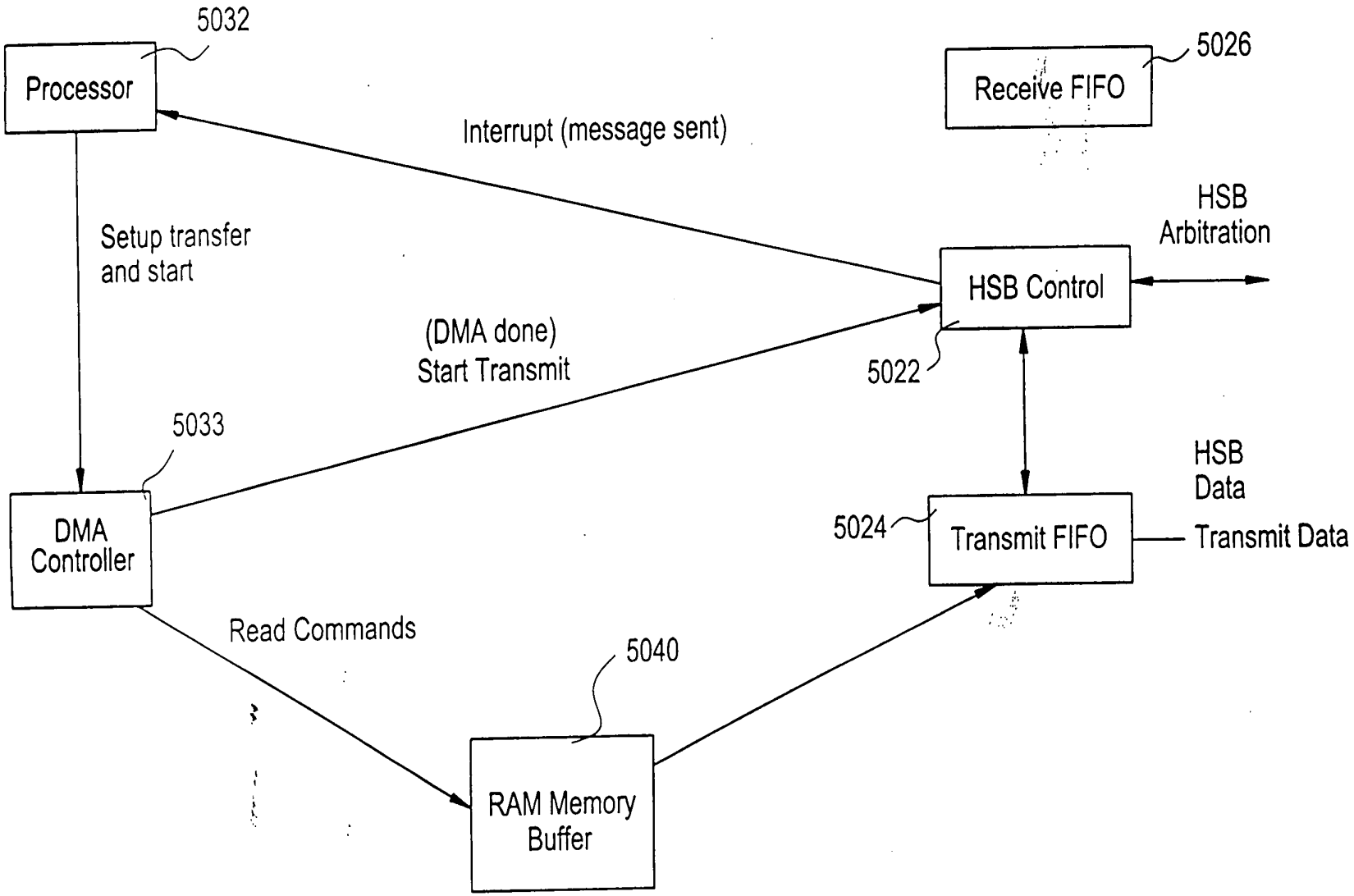

5032
Processor
Interrupt (message sent)
5026
Receive FIFO
HSB
Arbitration
Setup transfer
and start
HSB Control
(DMA done)
Start Transmit
5022
5033
HSB
Data
DMA
Controller
5024
Transmit FIFO
Transmit Data
Read Commands
5040
RAM Memory
Buffer

FIG. 59

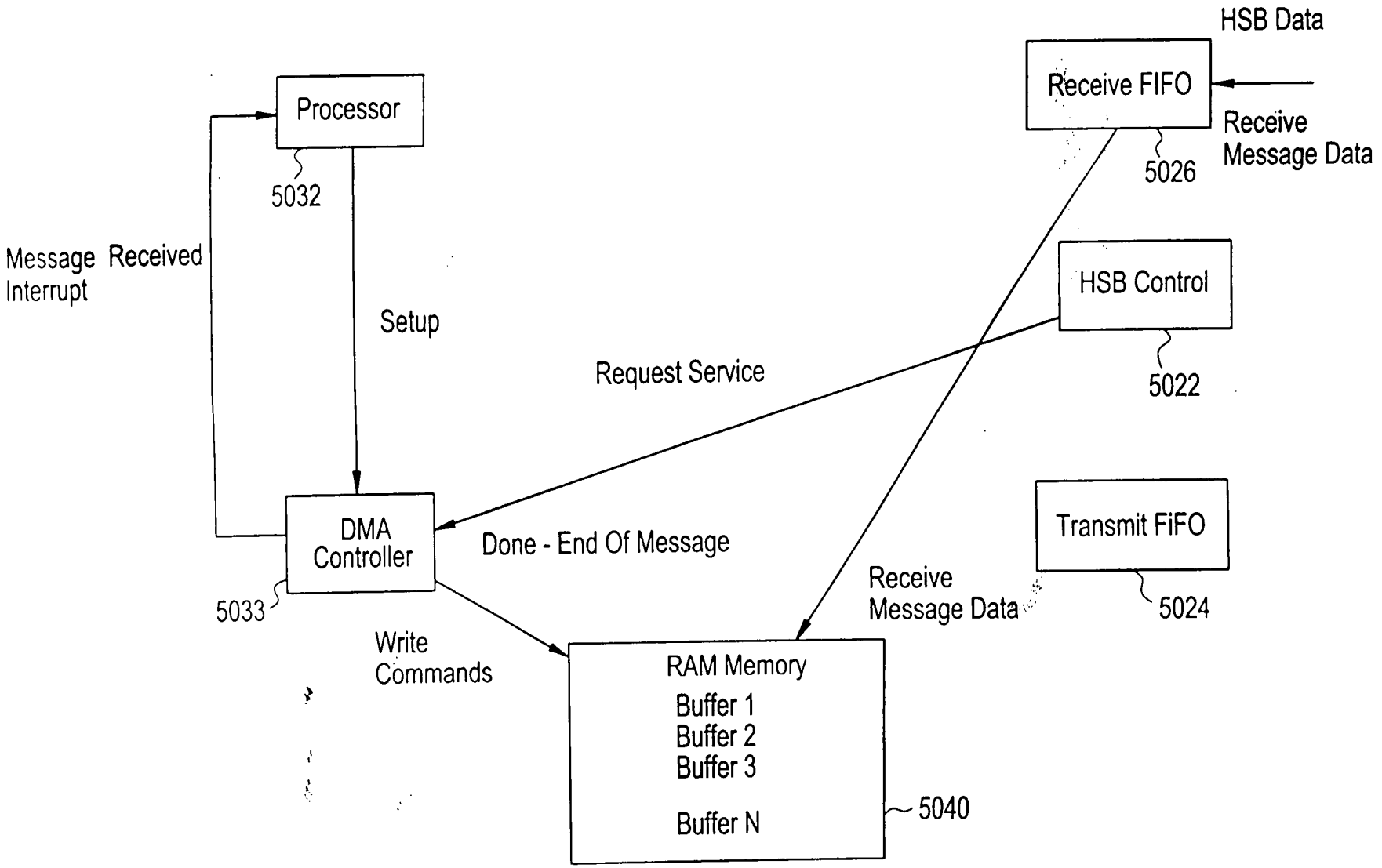

HSB Data
Receive FIFO
Receive
Message Data
5026
Processor
5032
Message Received
Interrupt
Setup
HSB Control
Request Service
5022
DMA
Controller
5033
Done - End Of Message
Transmit FiFO
Receive
Message Data
5024
Write
Commands
RAM Memory
Buffer 1
Buffer 2
Buffer 3
Buffer N
5040

FIG. 60

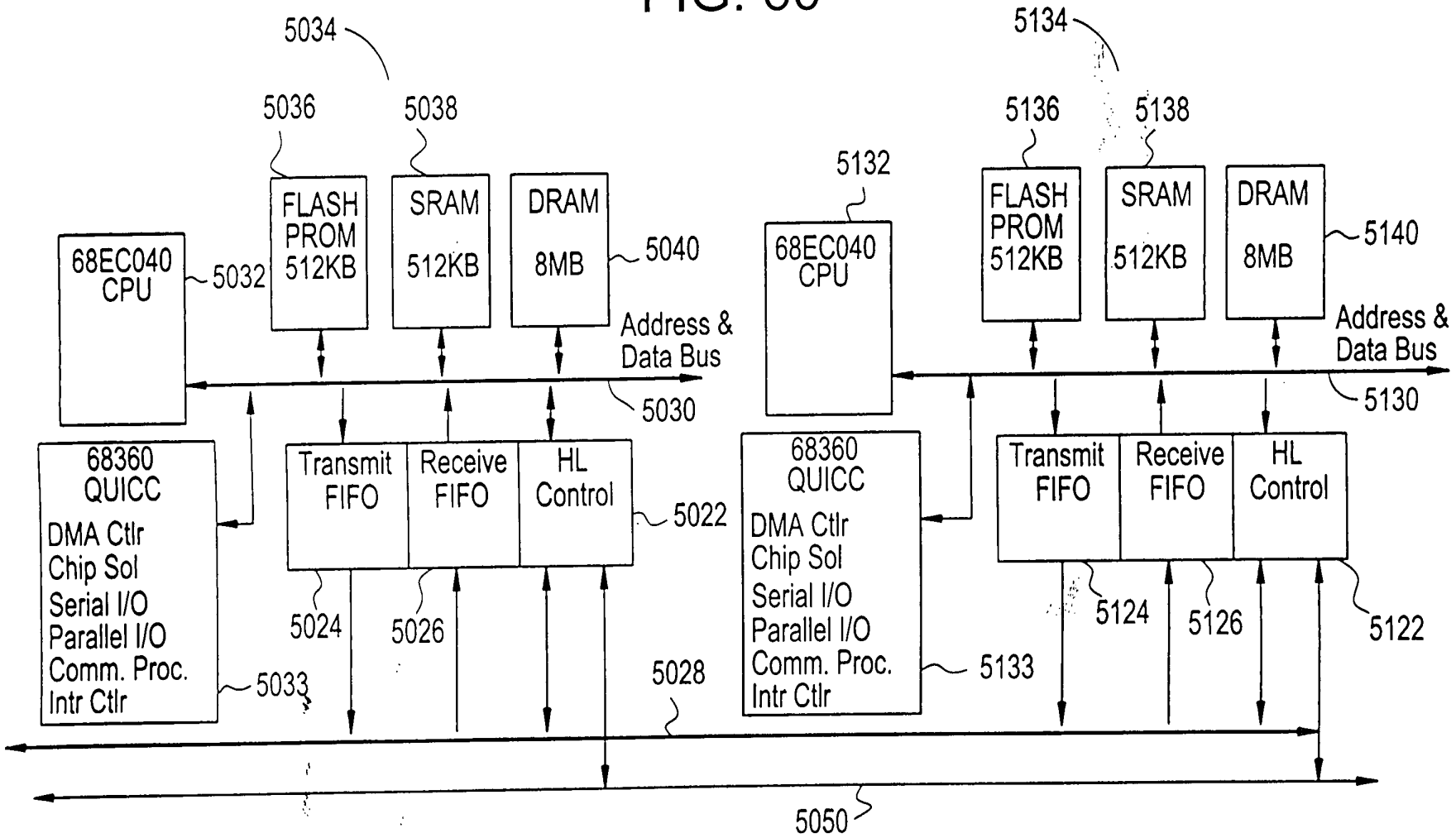

5034
5036
5038
5134
5136
5138
5132
FLASH PROM 512KB
SRAM 512KB
DRAM 8MB
5040
5140
68EC040 CPU
5032
Address & Data Bus
5030
5130
68360 QUICC
DMA Ctlr
Chip Sol
Serial I/O
Parallel I/O
Comm. Proc.
Intr Ctlr
5033
5133
Transmit FIFO
Receive FIFO
HL Control
5022
5024
5026
5028
5124
5126
5122
5050

FIG. 61

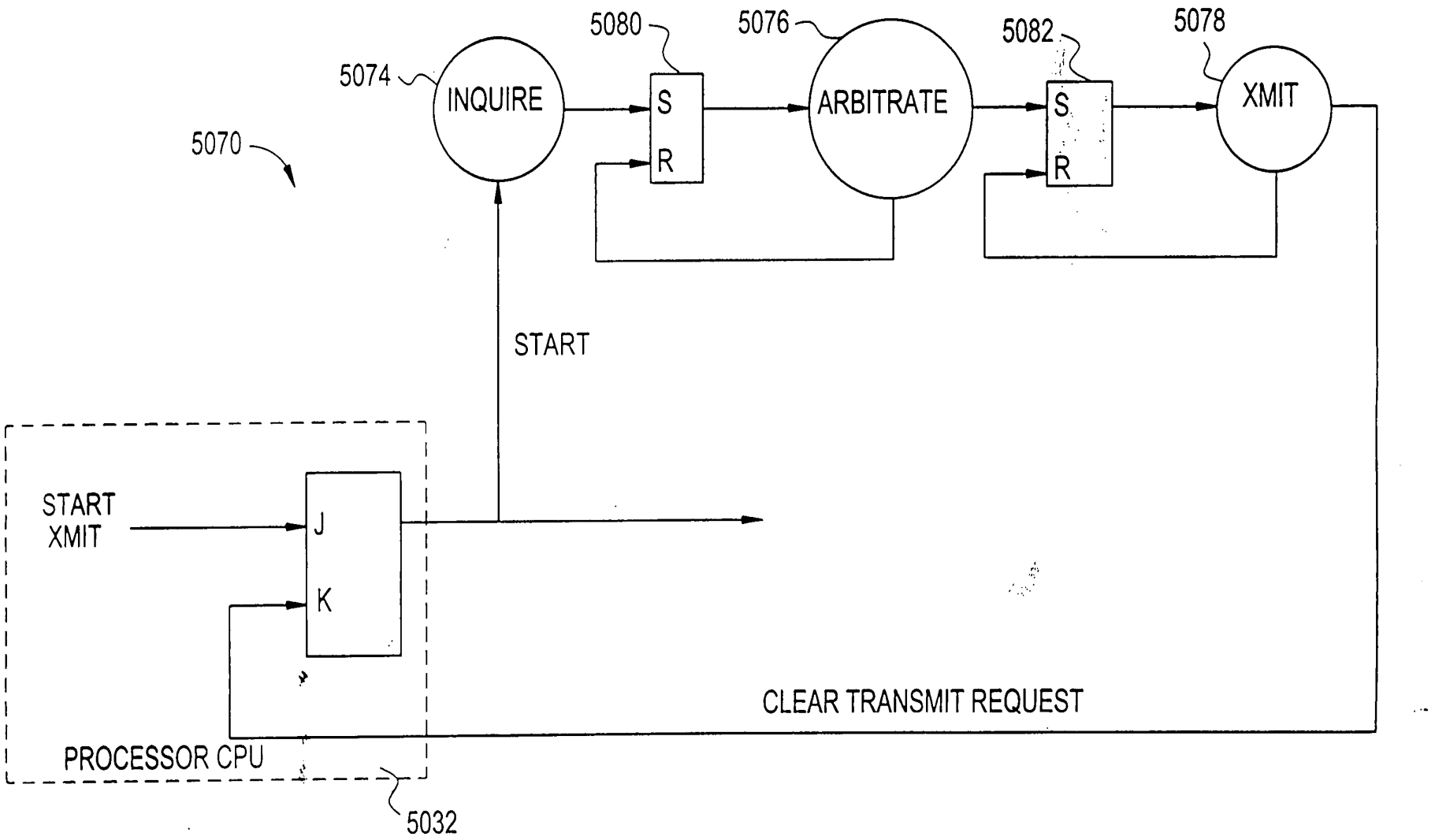

5070
5074
INQUIRE
5080
S
R
5076
ARBITRATE
5082
S
R
5078
XMIT
START
START XMIT
J
K
CLEAR TRANSMIT REQUEST
PROCESSOR CPU
5032

FIG. 62

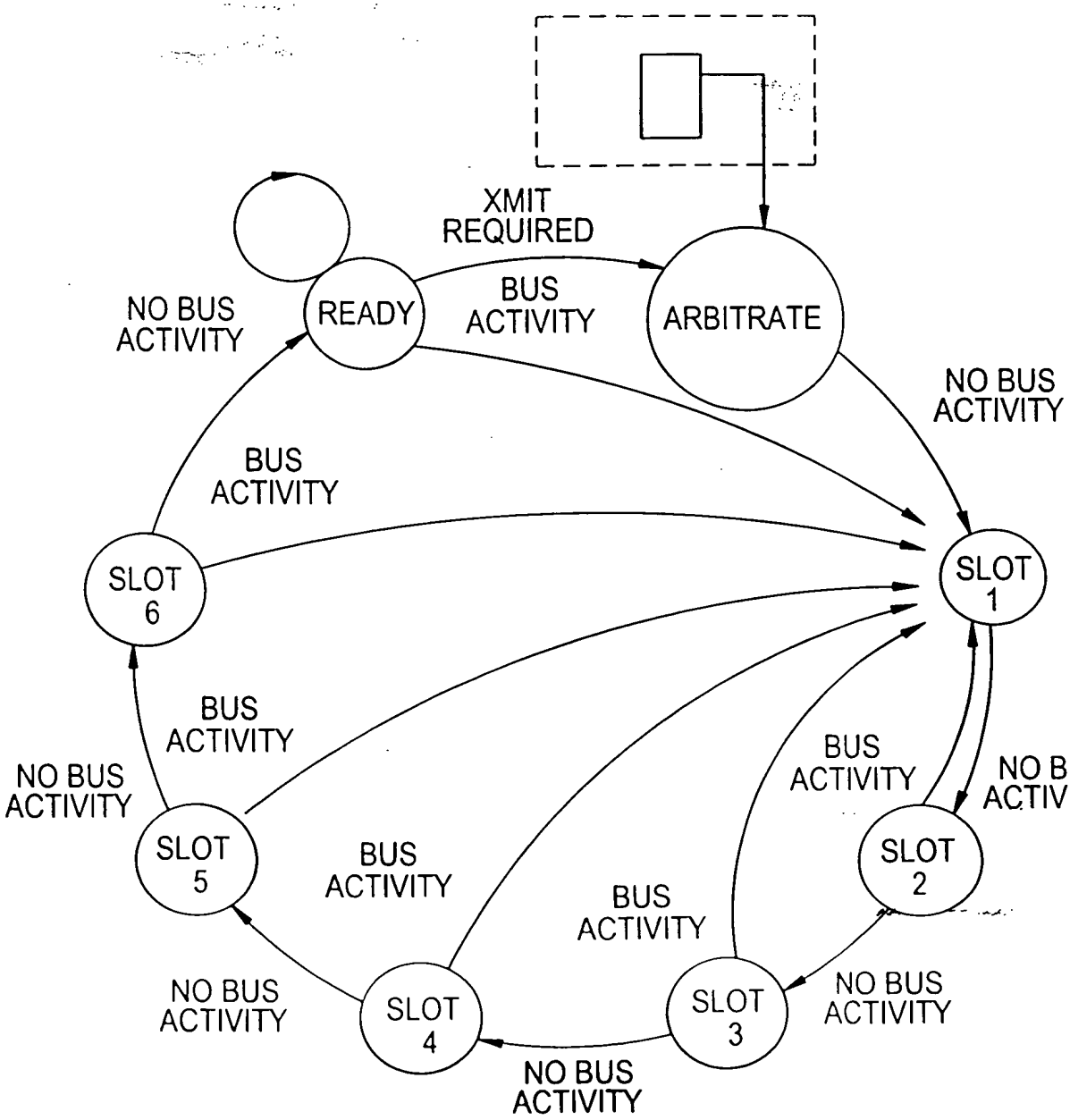

XMIT
REQUIRED
READY
BUS
ACTIVITY
ARBITRATE
NO BUS
ACTIVITY
NO BUS
ACTIVITY
BUS
ACTIVITY
SLOT
6
SLOT
1
BUS
ACTIVITY
NO BUS
ACTIVITY
BUS
ACTIVITY
NO BUS
ACTIVITY
SLOT
5
BUS
ACTIVITY
SLOT
2
BUS
ACTIVITY
NO BUS
ACTIVITY
SLOT
4
SLOT
3
NO BUS
ACTIVITY
NO BUS
ACTIVITY

FIG. 63

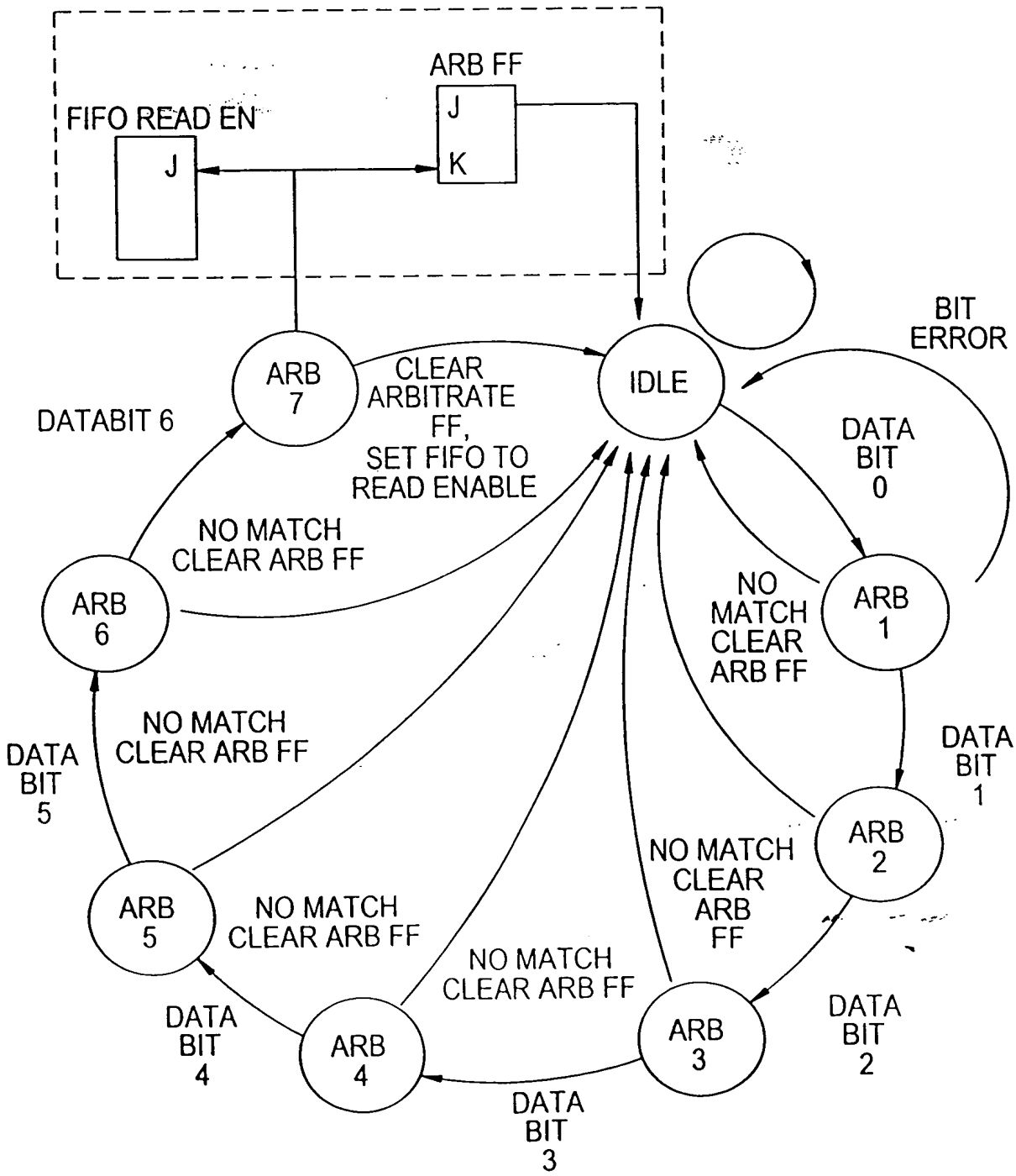

ARB FF
J
K
FIFO READ EN
J
IDLE
BIT ERROR
ARB 7
CLEAR ARBITRATE FF, SET FIFO TO READ ENABLE
DATABIT 6
DATA BIT 0
NO MATCH CLEAR ARB FF
ARB 6
ARB 1
NO MATCH CLEAR ARB FF
DATA BIT 1
DATA BIT 5
NO MATCH CLEAR ARB FF
ARB 2
ARB 5
NO MATCH CLEAR ARB FF
NO MATCH CLEAR ARB FF
NO MATCH CLEAR ARB FF
DATA BIT 4
ARB 4
ARB 3
DATA BIT 2
DATA BIT 3

FIG. 64

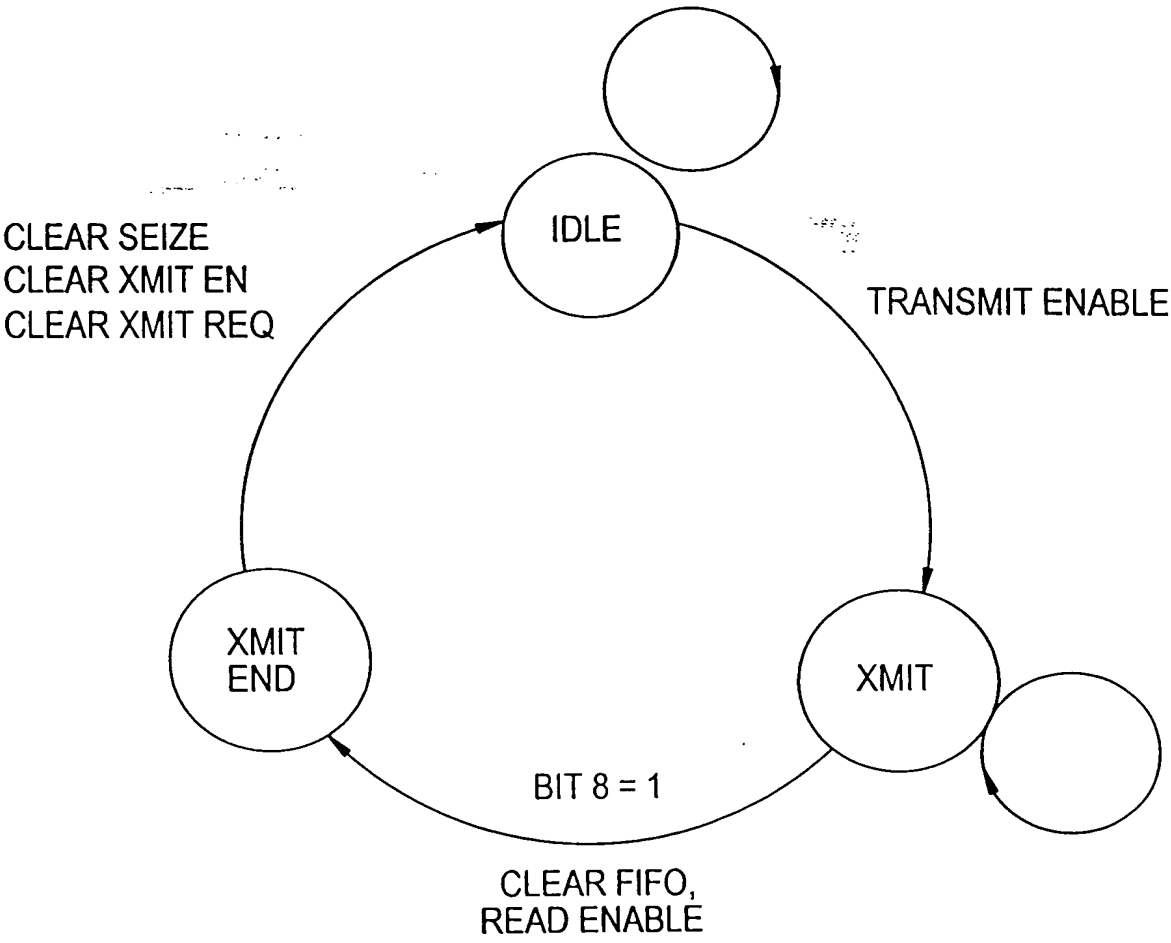

IDLE
CLEAR SEIZE
CLEAR XMIT EN
CLEAR XMIT REQ
TRANSMIT ENABLE
XMIT
END
XMIT
BIT 8 = 1
CLEAR FIFO,
READ ENABLE

FIG. 65

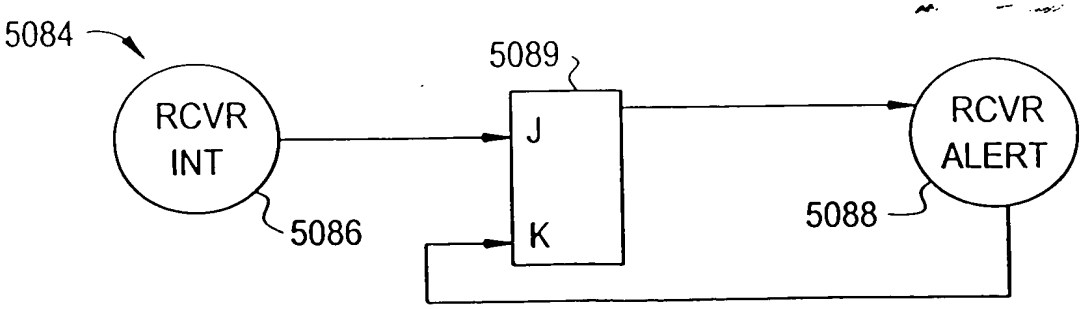

5084
RCVR
INT
5086
5089
J
K
RCVR
ALERT
5088

FIG. 66

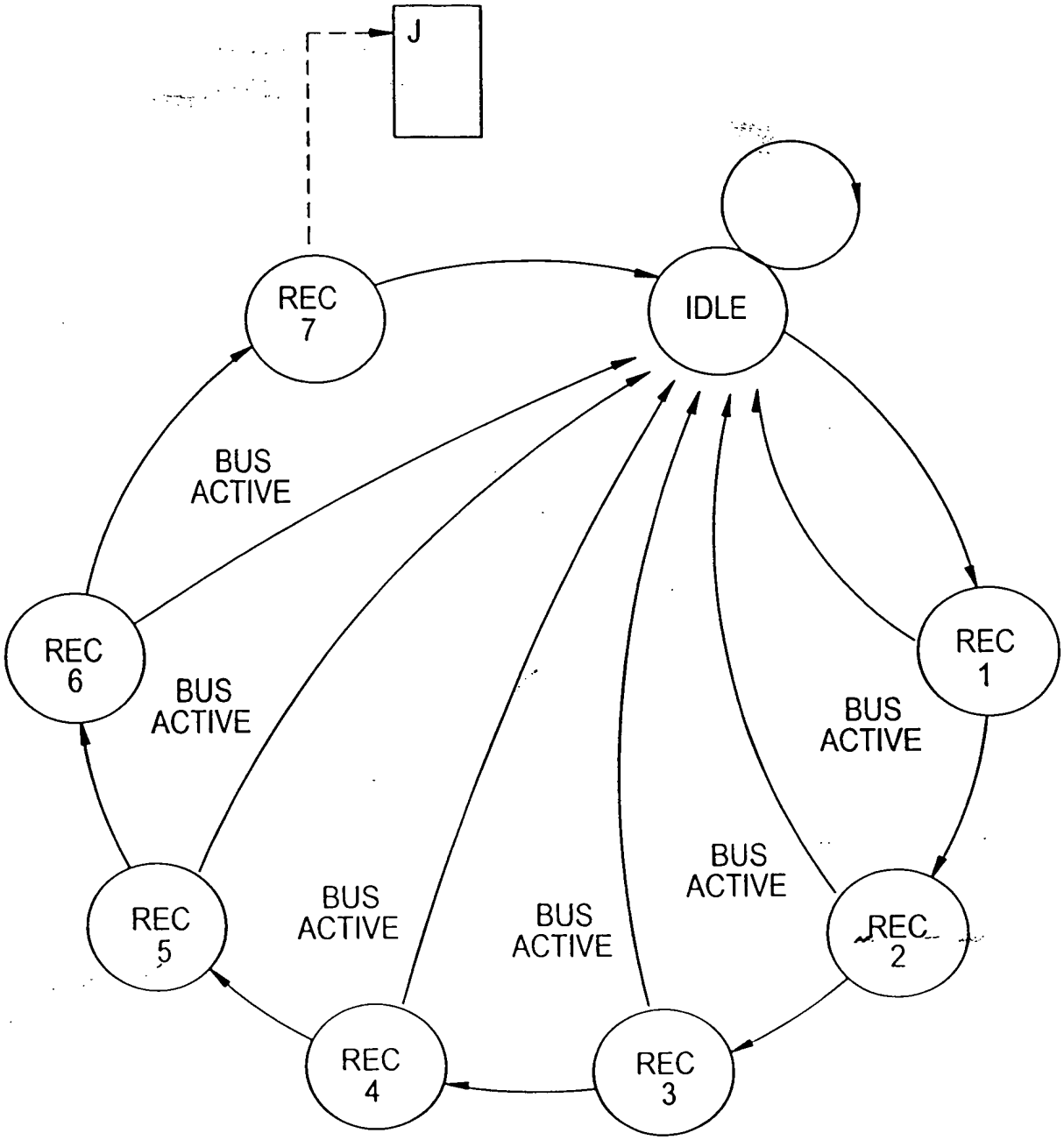

J
IDLE
REC 7
REC 1
REC 2
REC 3
REC 4
REC 5
REC 6
BUS ACTIVE
BUS ACTIVE
BUS ACTIVE
BUS ACTIVE
BUS ACTIVE
BUS ACTIVE

FIG. 67

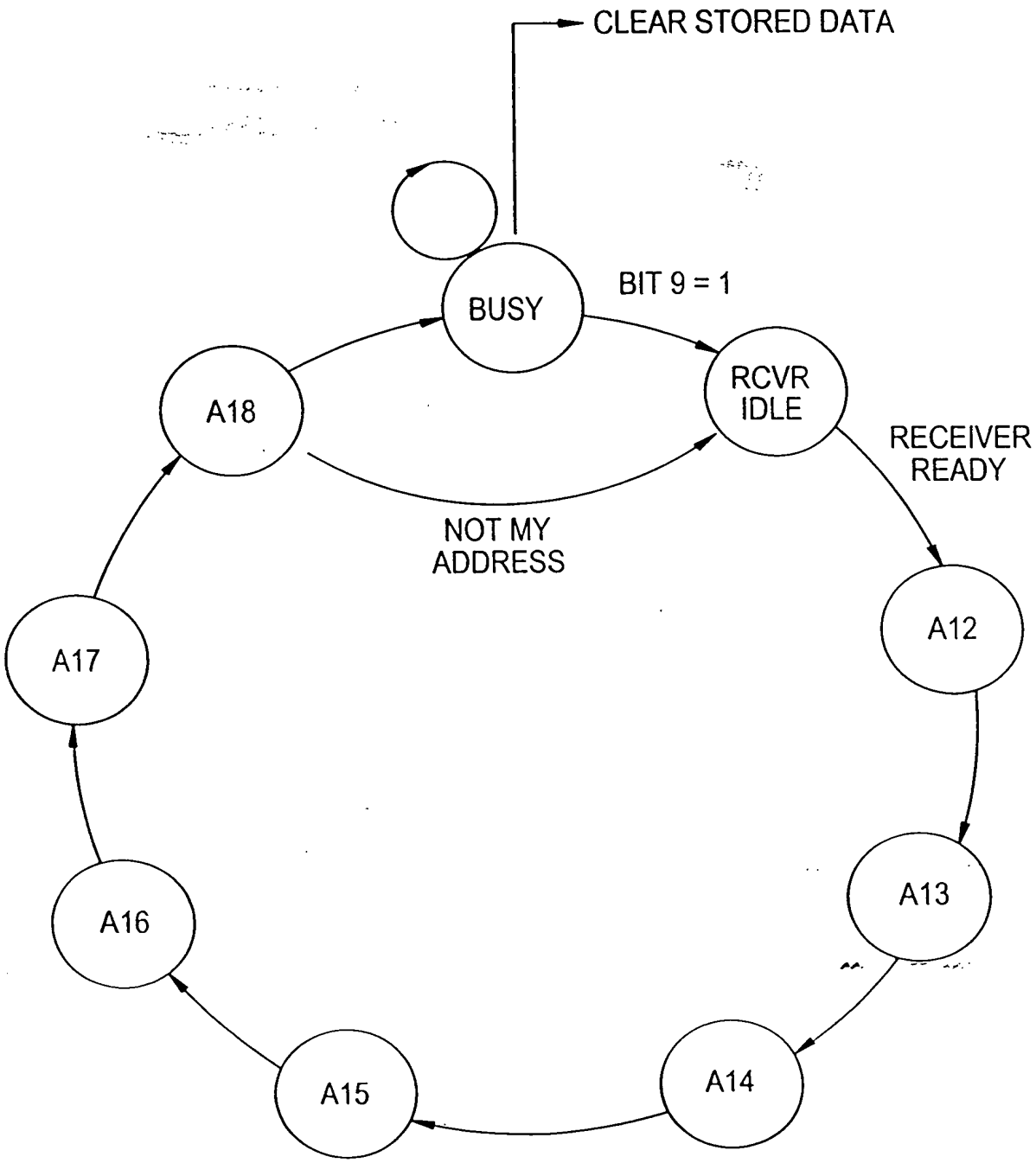

CLEAR STORED DATA
BUSY
BIT 9 = 1
RCVR IDLE
RECEIVER READY
A12
A13
A14
A15
A16
A17
A18
NOT MY ADDRESS

FIG. 68

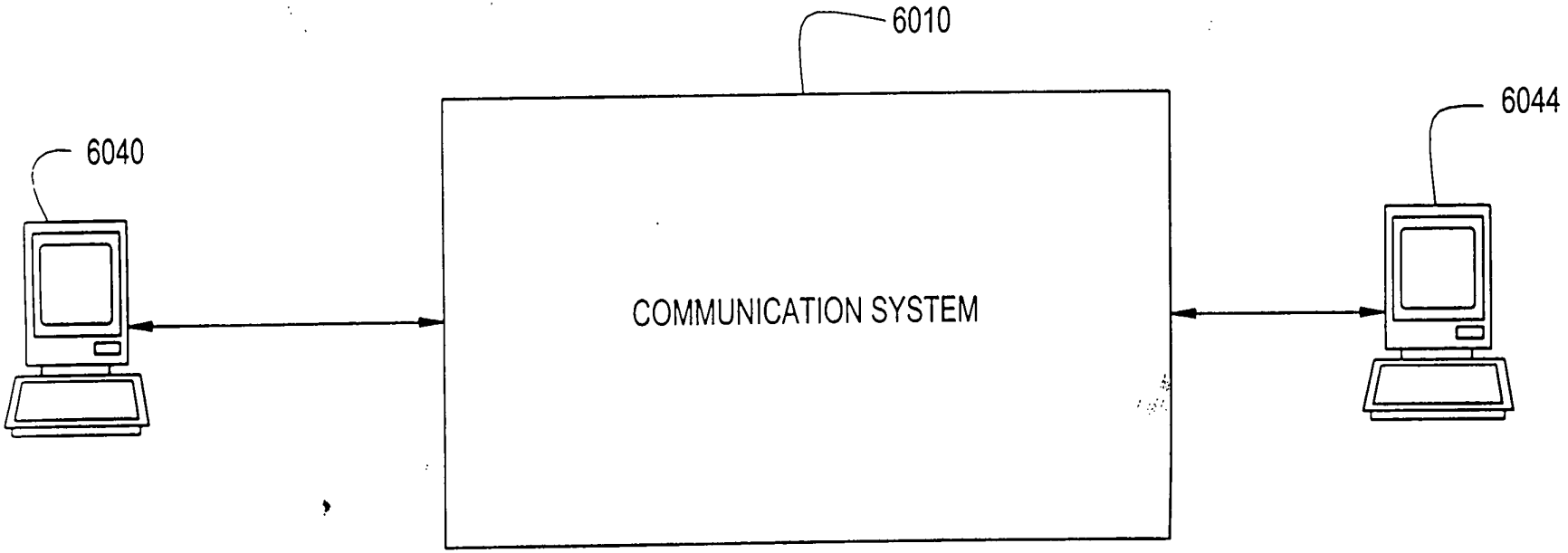


FIG. 69
PRIOR ART

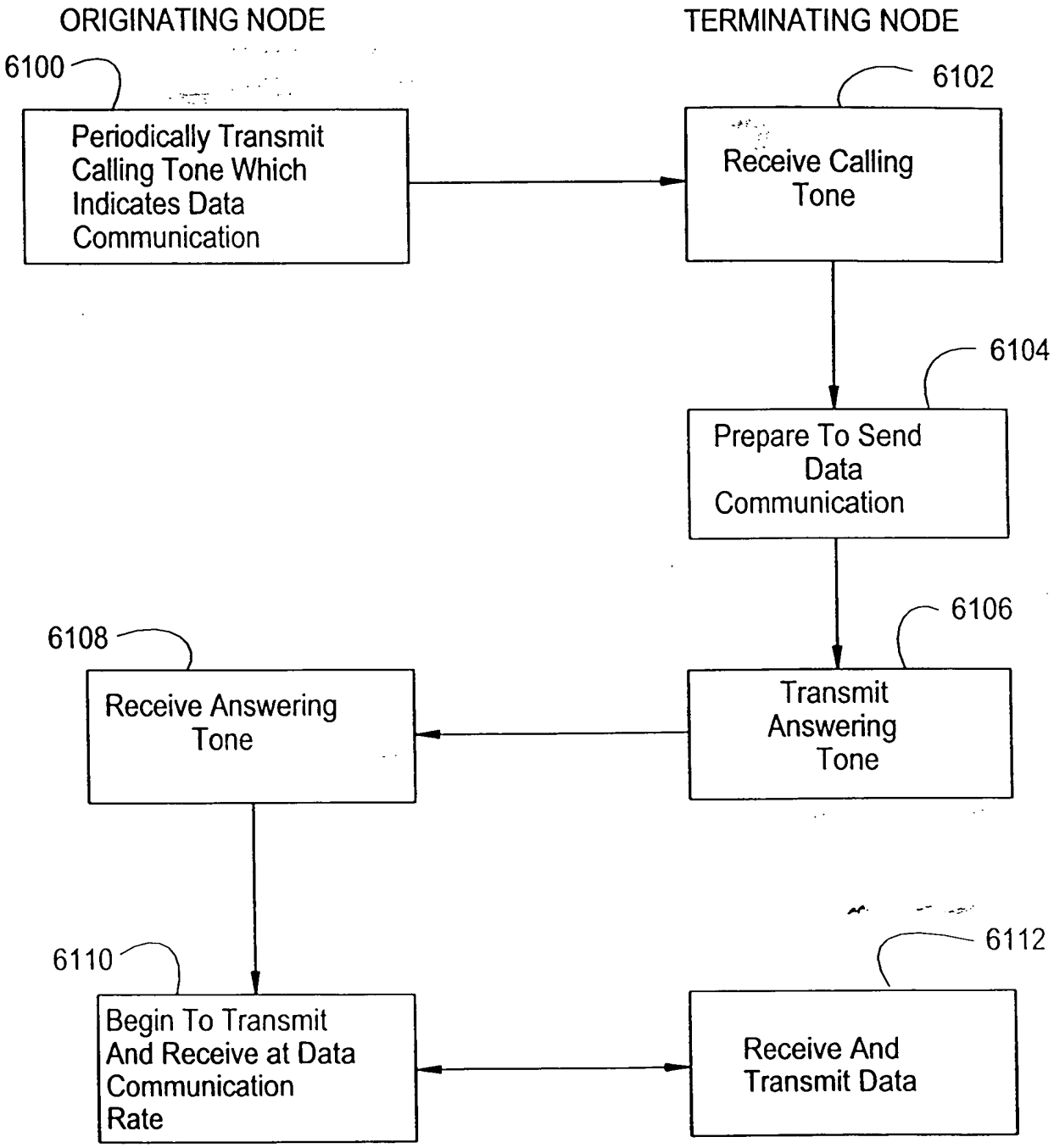


FIG. 70

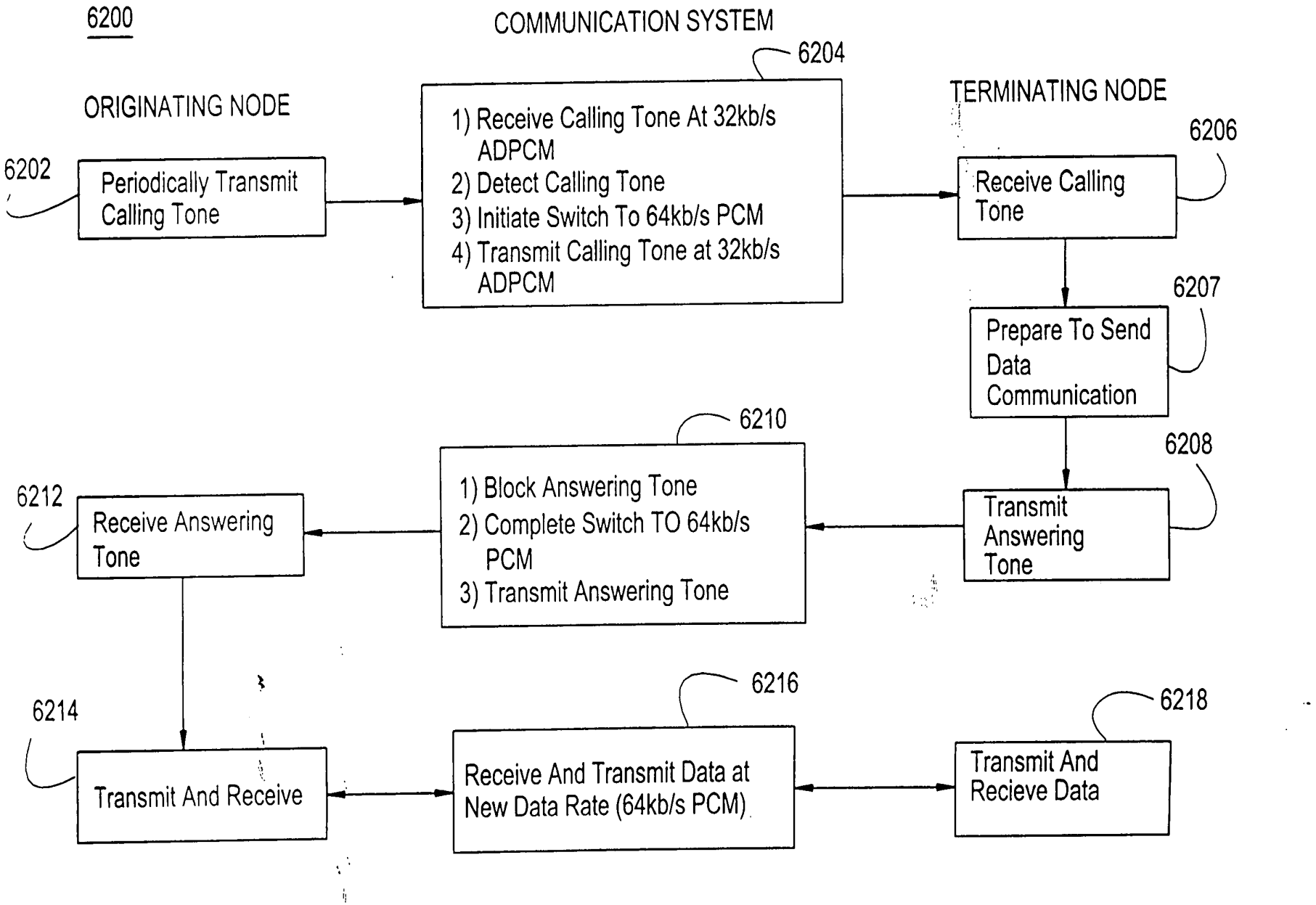

6200
COMMUNICATION SYSTEM
6204
ORIGINATING NODE
TERMINATING NODE
6202
Periodically Transmit Calling Tone
1) Receive Calling Tone At 32kb/s ADPCM
2) Detect Calling Tone
3) Initiate Switch To 64kb/s PCM
4) Transmit Calling Tone at 32kb/s ADPCM
6206
Receive Calling Tone
6207
Prepare To Send Data Communication
6208
Transmit Answering Tone
6210
1) Block Answering Tone
2) Complete Switch TO 64kb/s PCM
3) Transmit Answering Tone
6212
Receive Answering Tone
6214
Transmit And Receive
6216
Receive And Transmit Data at New Data Rate (64kb/s PCM)
6218
Transmit And Recieve Data

FIG. 71

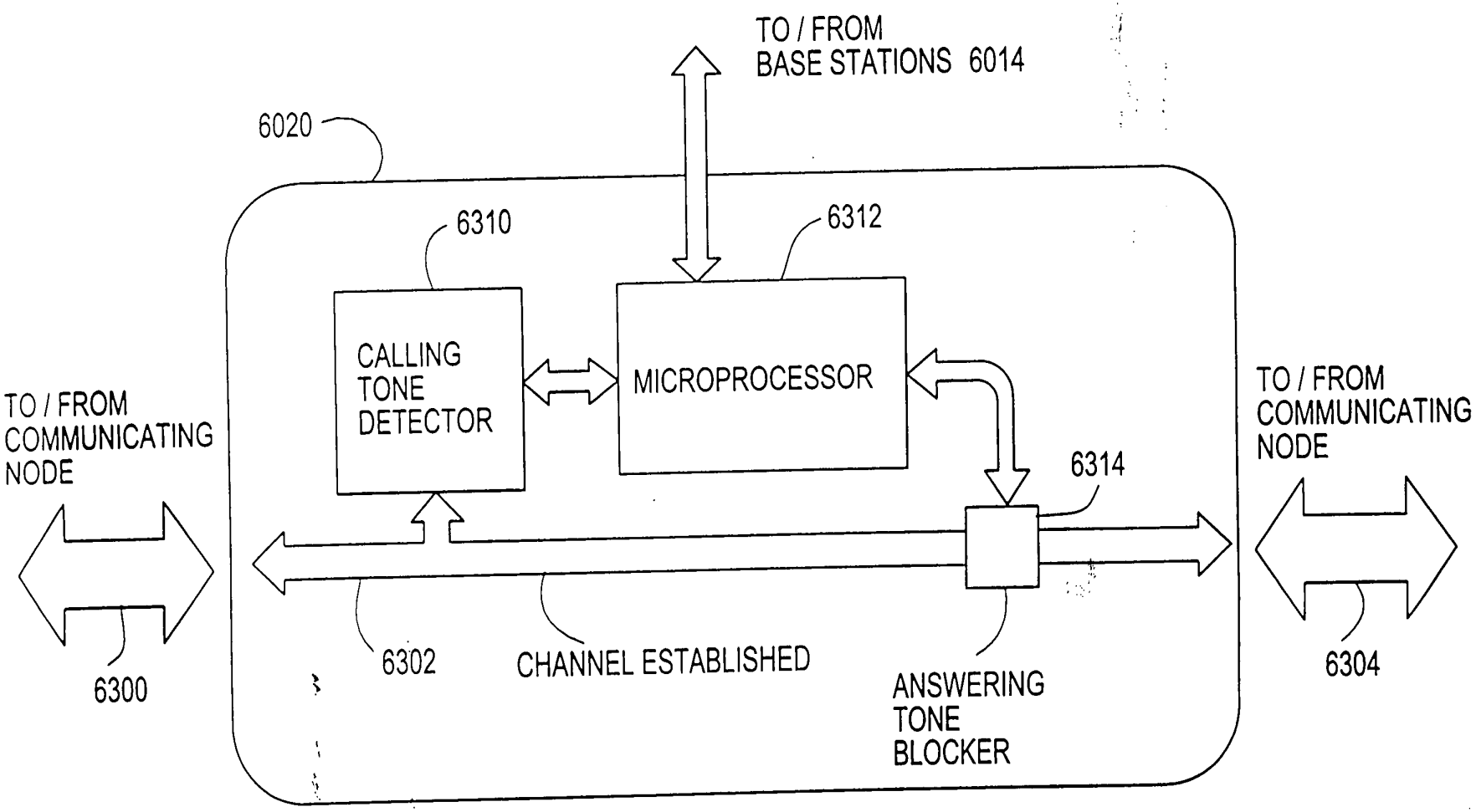

TO / FROM
BASE STATIONS 6014
6020
6310
6312
CALLING
TONE
DETECTOR
MICROPROCESSOR
TO / FROM
COMMUNICATING
NODE
6314
TO / FROM
COMMUNICATING
NODE
6302
CHANNEL ESTABLISHED
ANSWERING
TONE
BLOCKER
6300
6304

FIG. 72
PRIOR ART

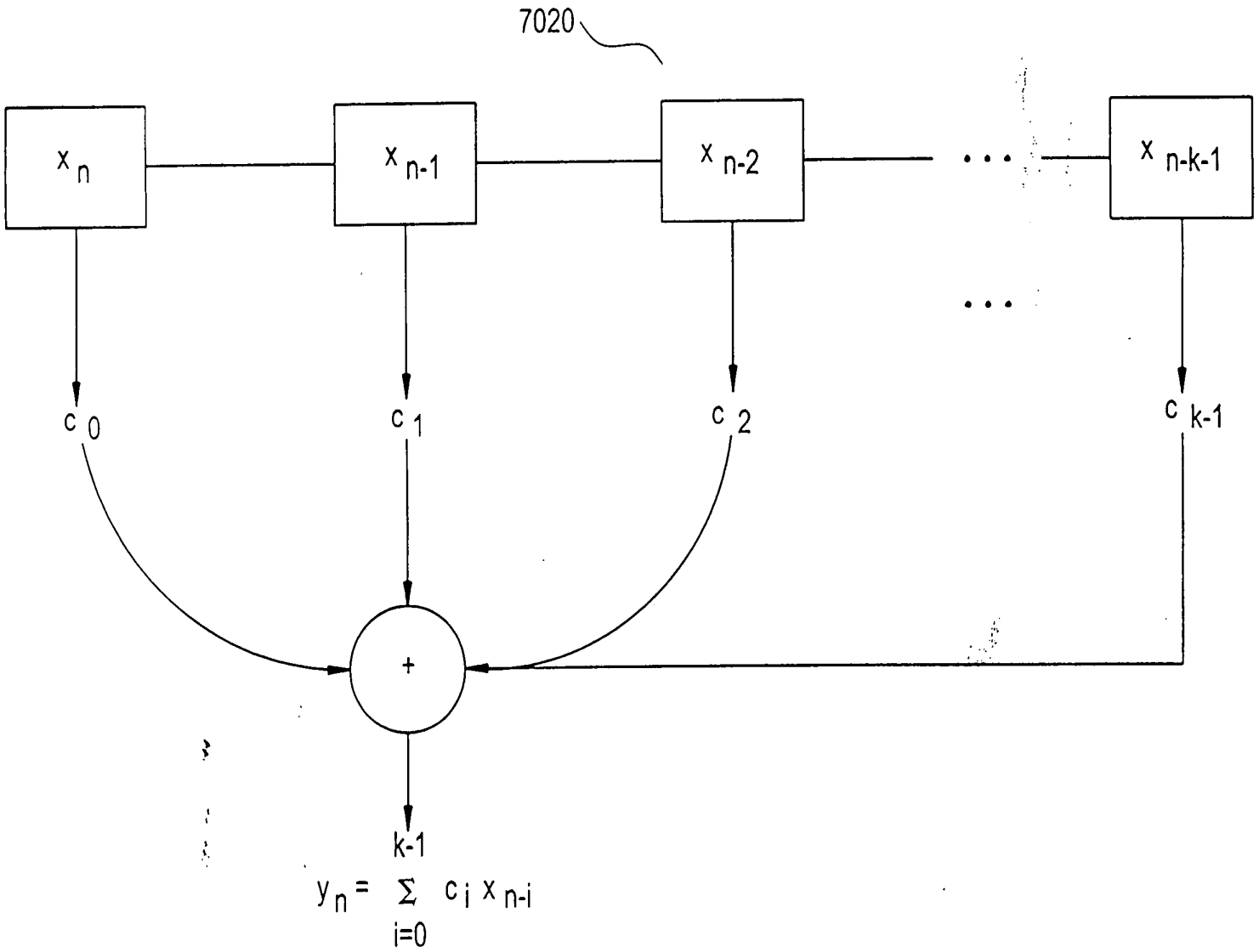


FIG. 73
PRIOR ART

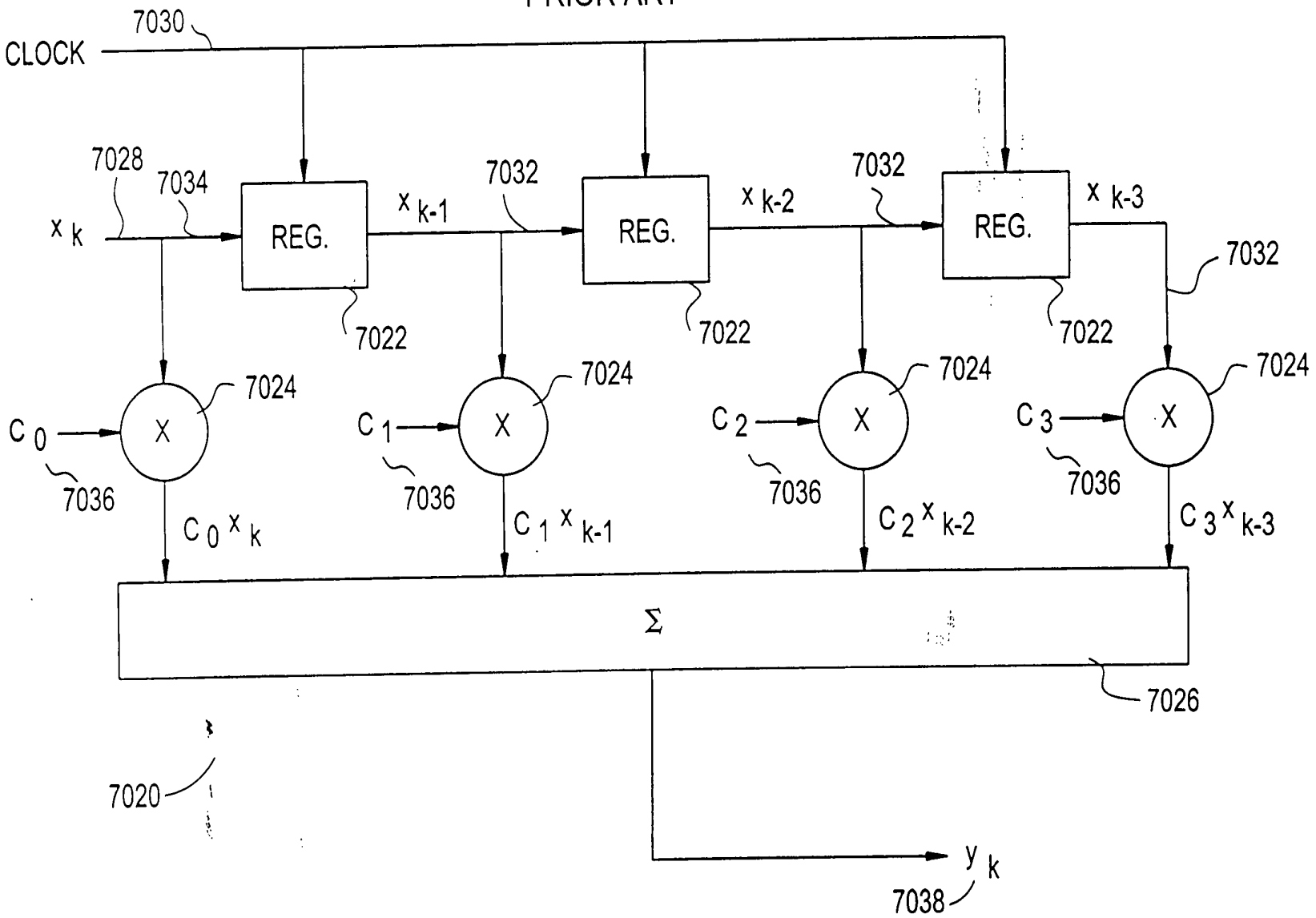


FIG. 74
PRIOR ART

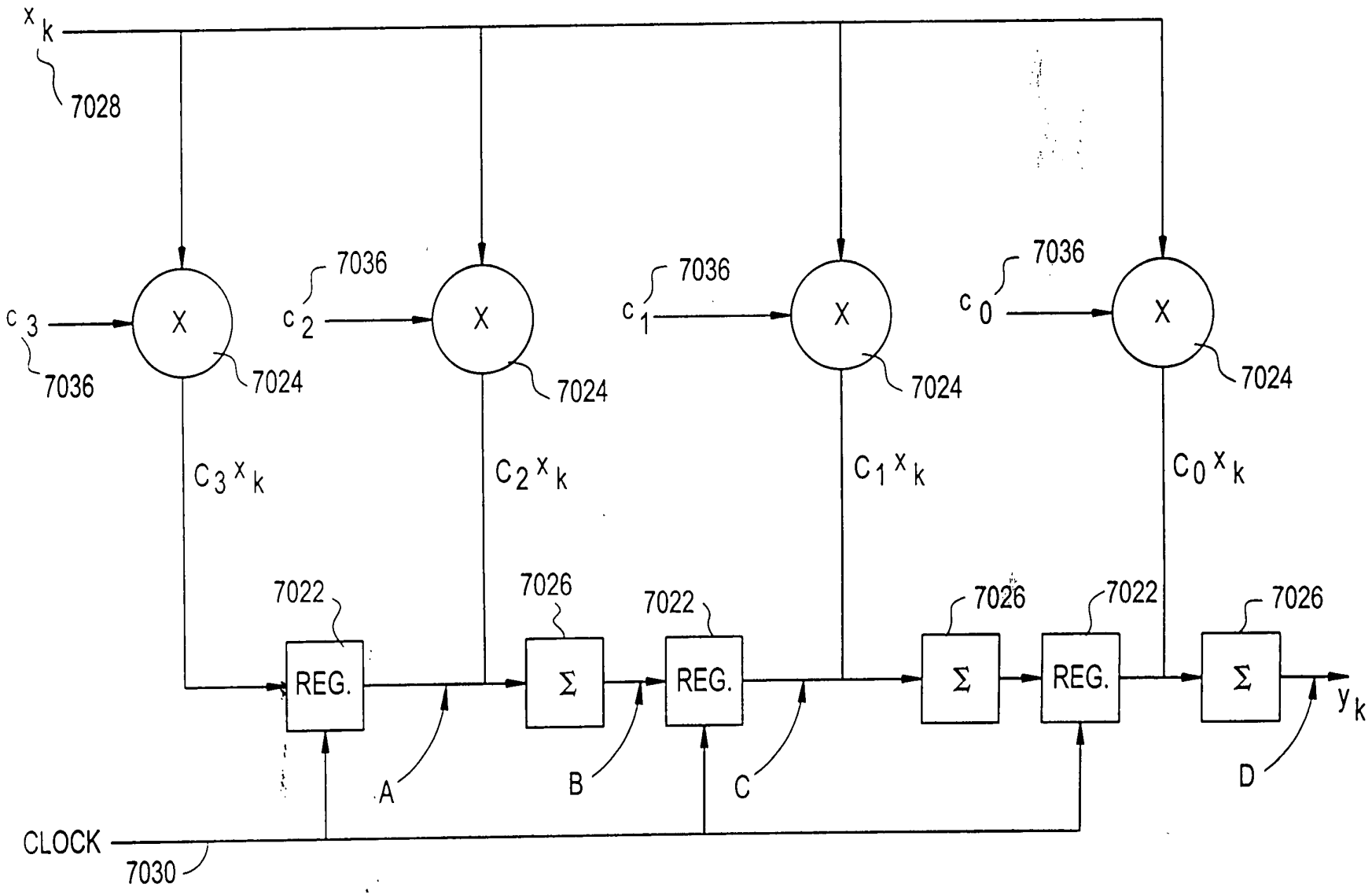
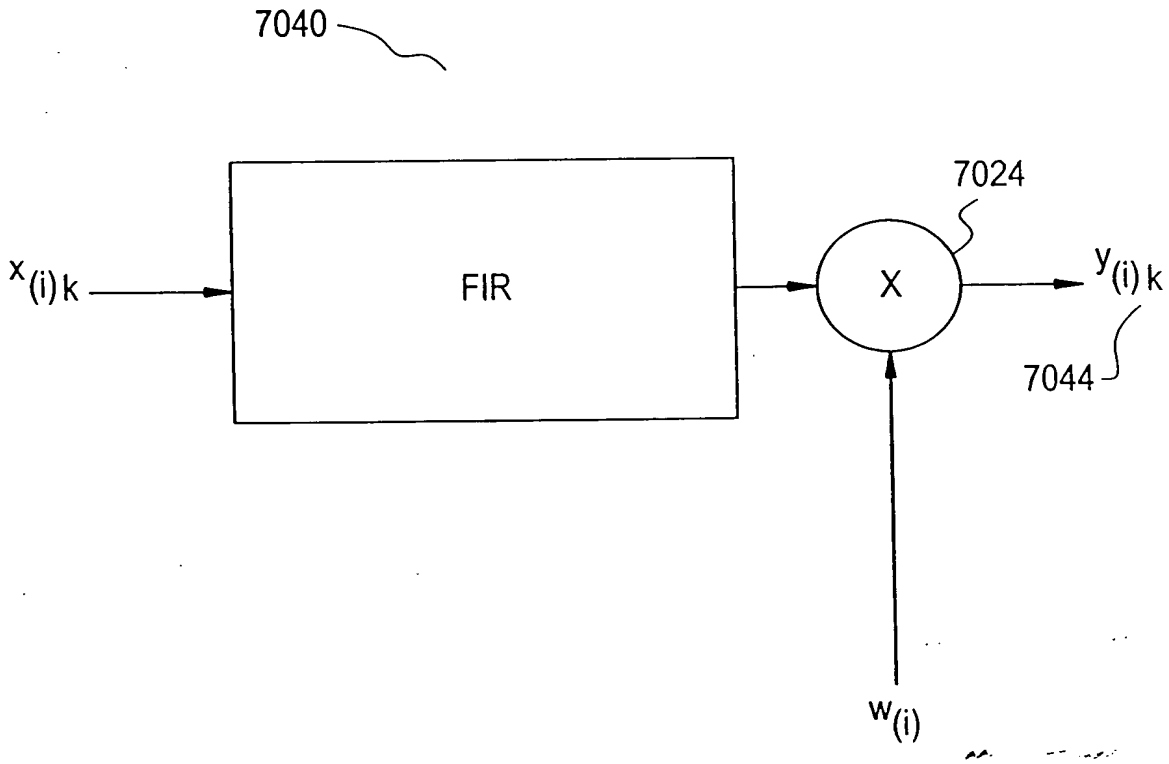


FIG. 75A



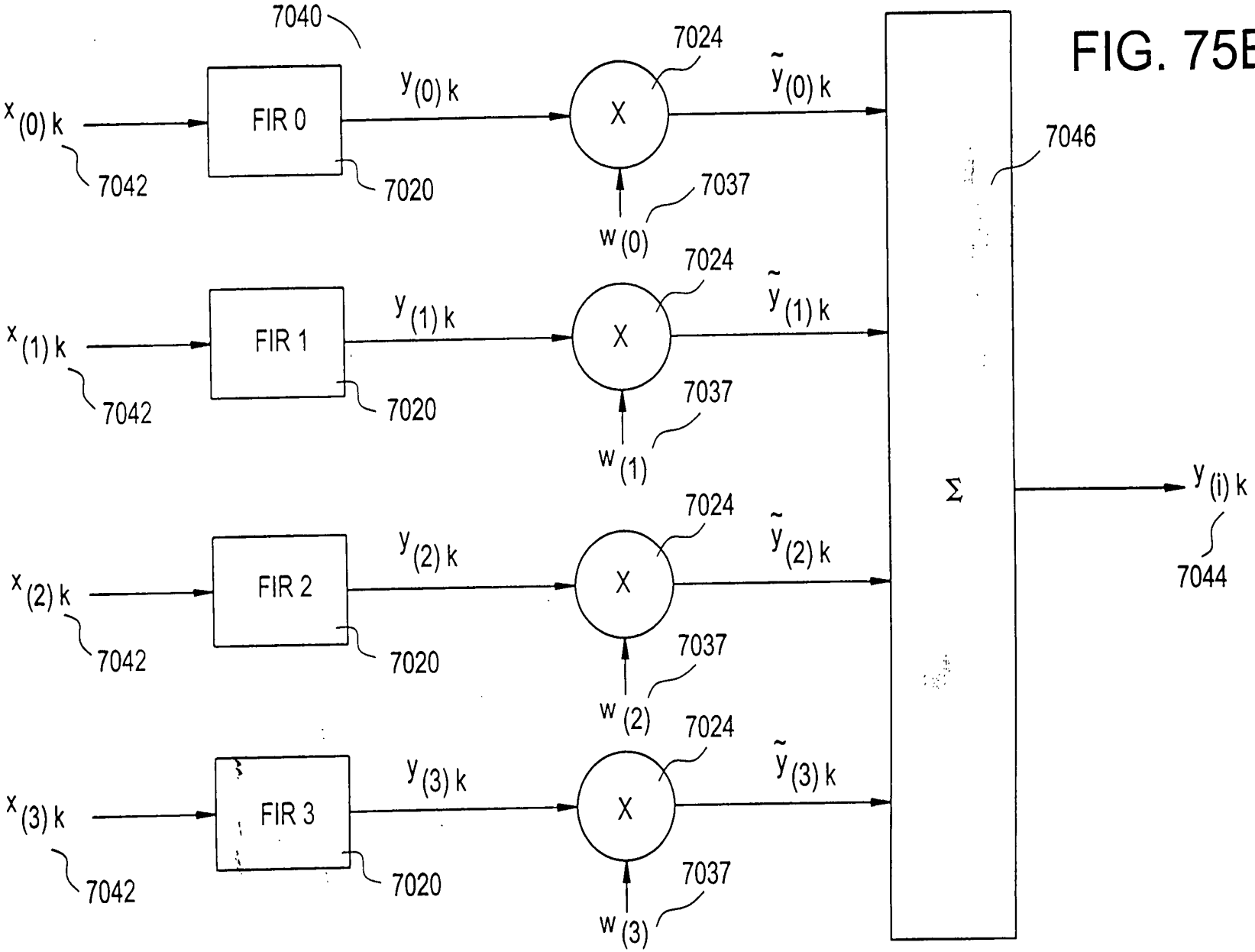

7040
FIR 0
FIR 1
FIR 2
FIR 3
x (0) k
x (1) k
x (2) k
x (3) k
7042
7020
y (0) k
y (1) k
y (2) k
y (3) k
X
7024
w (0)
w (1)
w (2)
w (3)
7037
ỹ (0) k
ỹ (1) k
ỹ (2) k
ỹ (3) k
Σ
7046
y (i) k
7044

FIG. 75B

FIG. 76

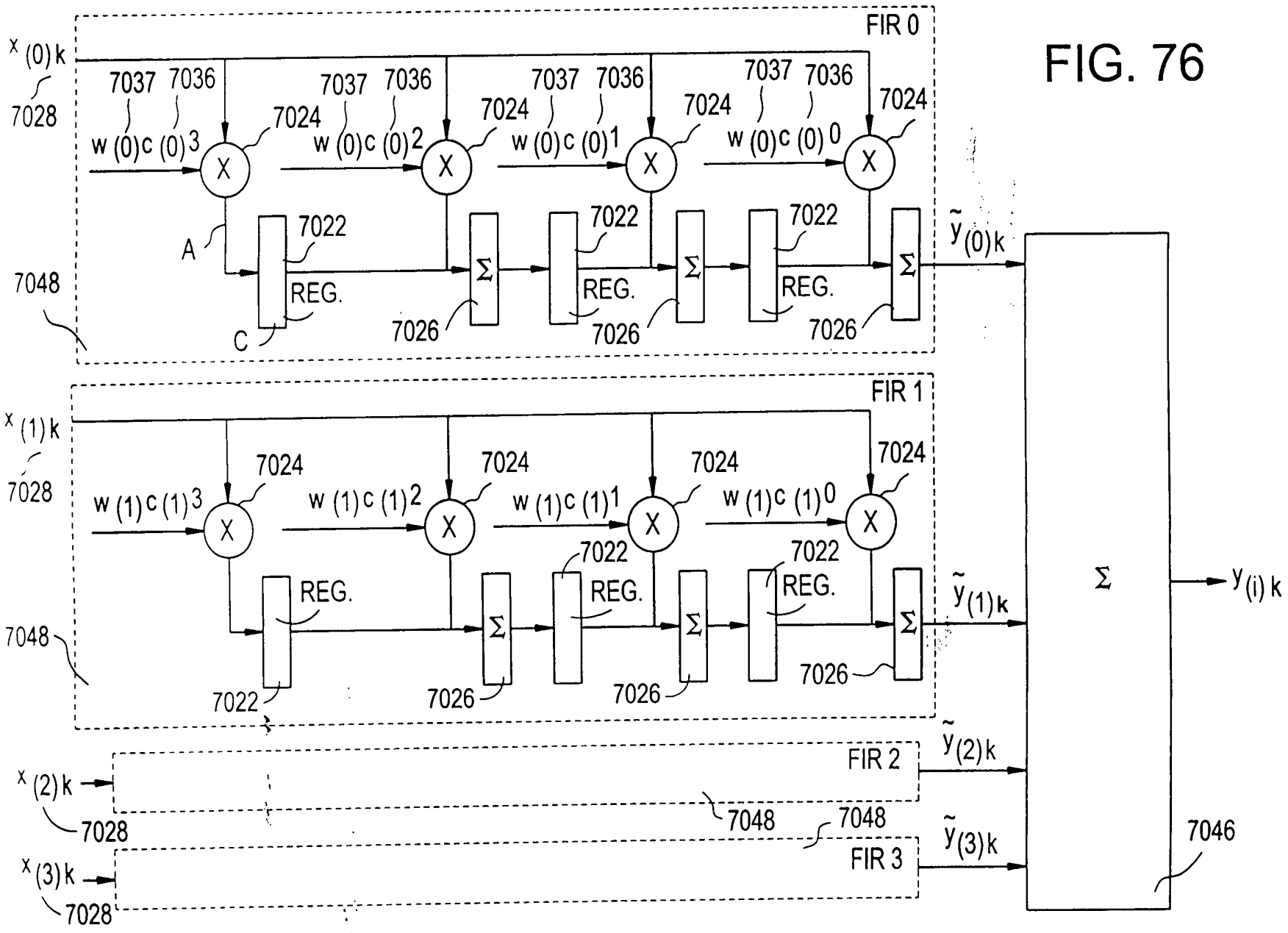

FIR 0
FIR 1
FIR 2
FIR 3
x (0) k
x (1) k
x (2) k
x (3) k
7028
7037
7036
7024
w (0) c (0) 3
w (0) c (0) 2
w (0) c (0) 1
w (0) c (0) 0
w (1) c (1) 3
w (1) c (1) 2
w (1) c (1) 1
w (1) c (1) 0
X
A
C
7022
REG.
7026
Σ
7048
ỹ (0) k
ỹ (1) k
ỹ (2) k
ỹ (3) k
y (i) k
7046

FIG. 77

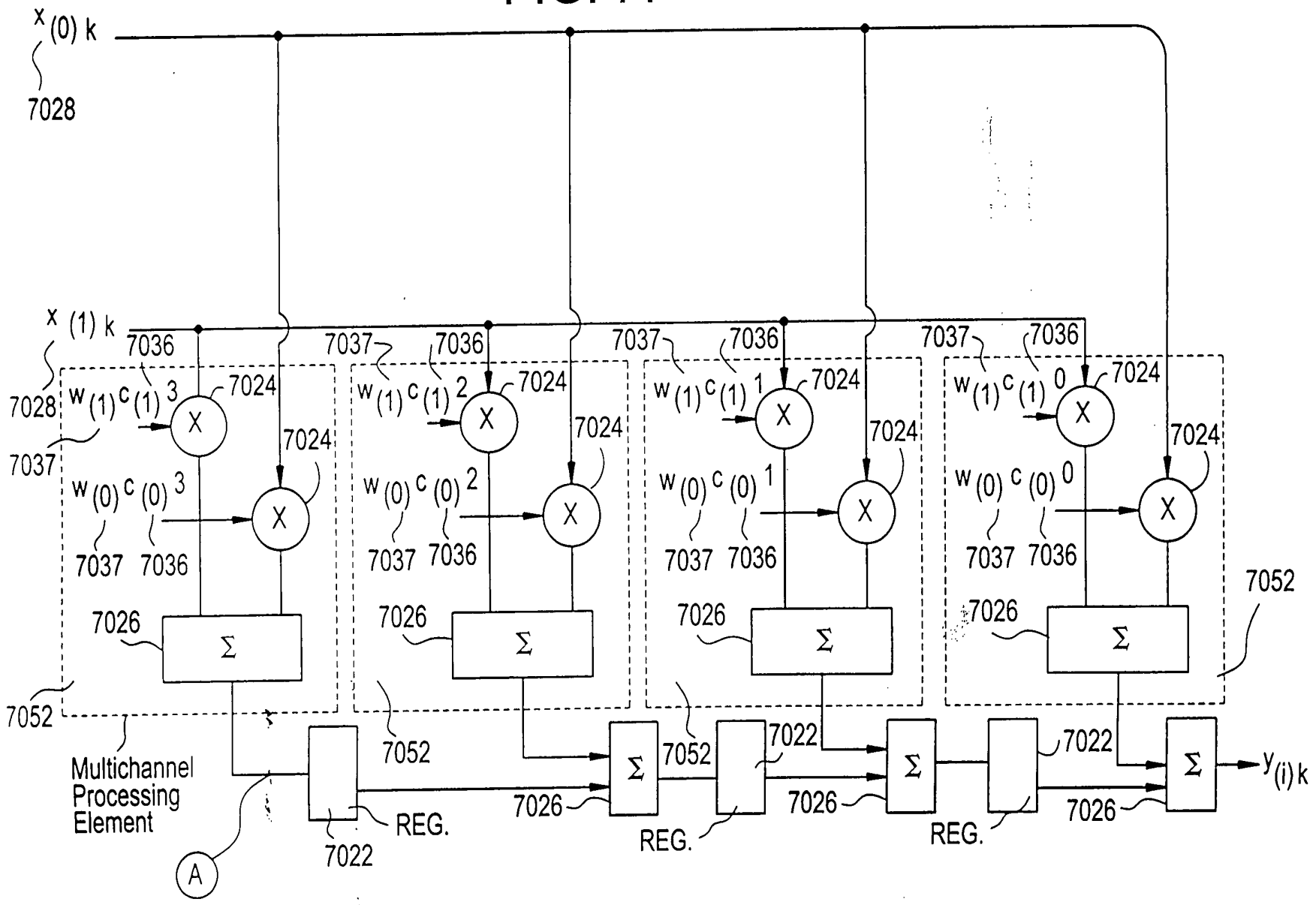

x (0) k
7028
x (1) k
7028
7036
7037
7024
w (1) c (1) 3
w (0) c (0) 3
7037 7036
7026
Σ
7052
Multichannel Processing Element
A
7022
REG.
w (1) c (1) 2
w (0) c (0) 2
w (1) c (1) 1
w (0) c (0) 1
w (1) c (1) 0
w (0) c (0) 0
y (i) k

FIG. 78

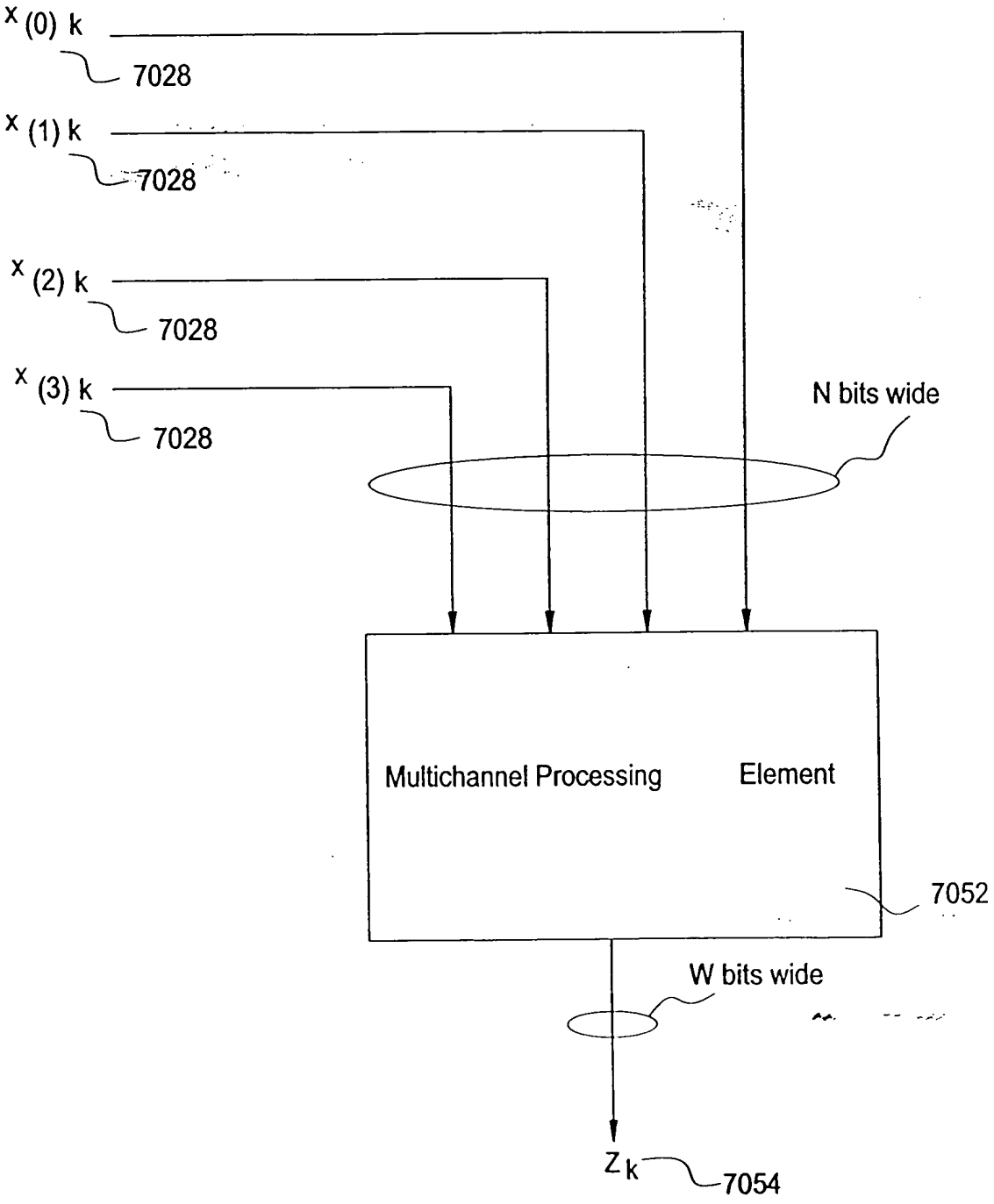

x (0) k
7028
x (1) k
7028
x (2) k
7028
x (3) k
7028
N bits wide
Multichannel Processing Element
7052
W bits wide
Z k
7054

FIG. 79A

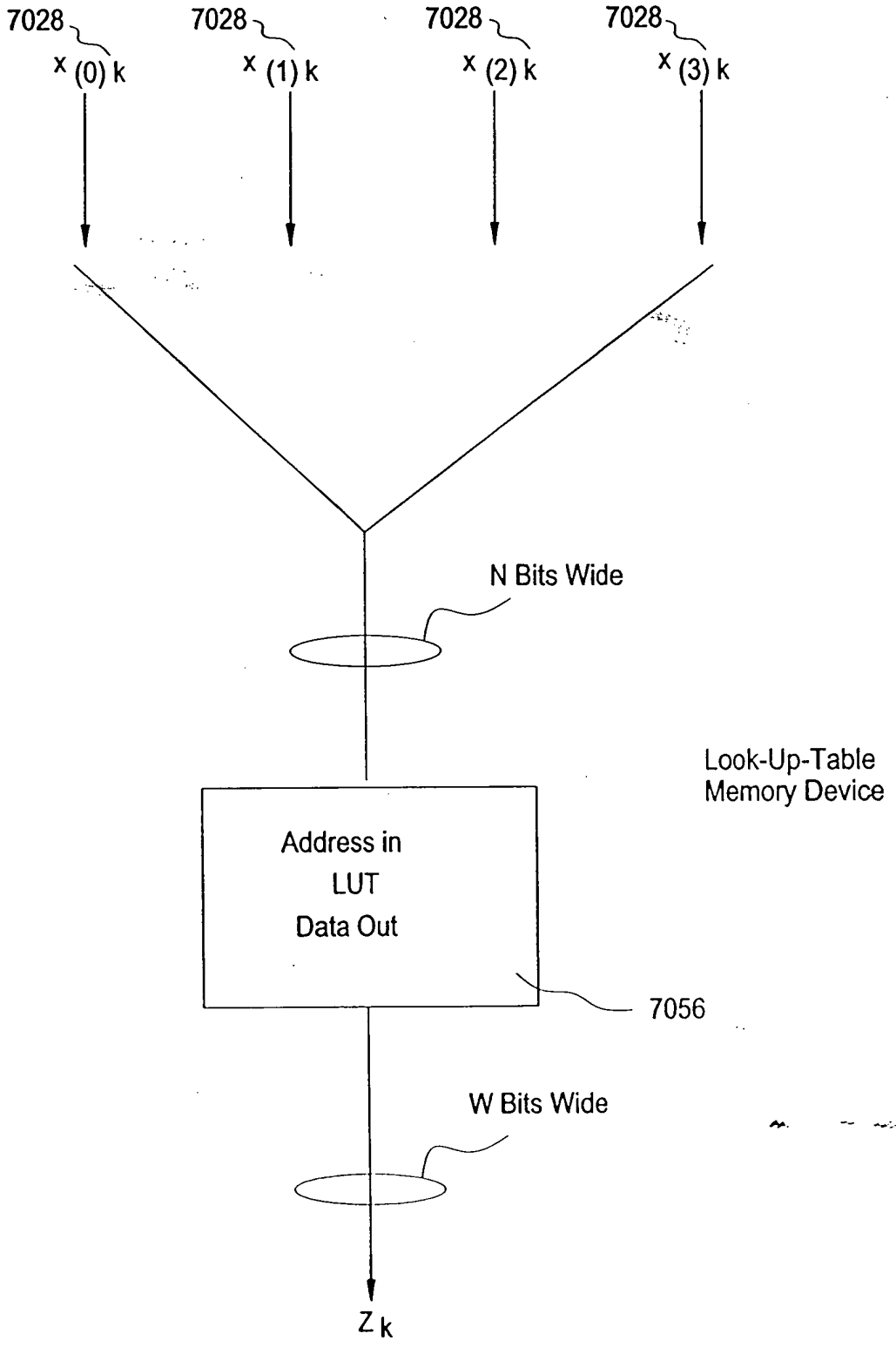

7028
x (0) k
7028
x (1) k
7028
x (2) k
7028
x (3) k
N Bits Wide
Look-Up-Table
Memory Device
Address in
LUT
Data Out
7056
W Bits Wide
Z k

FIG. 79B

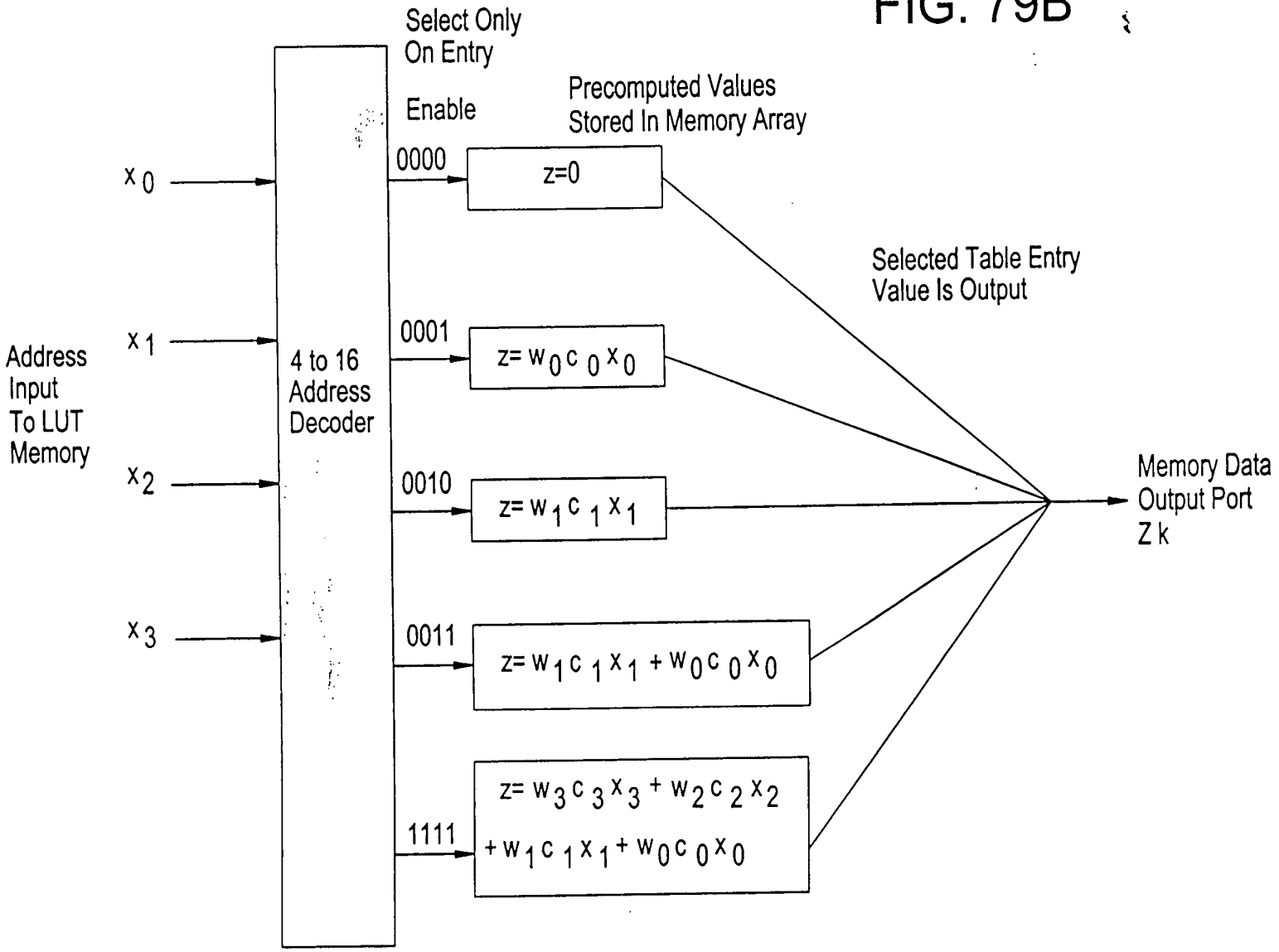
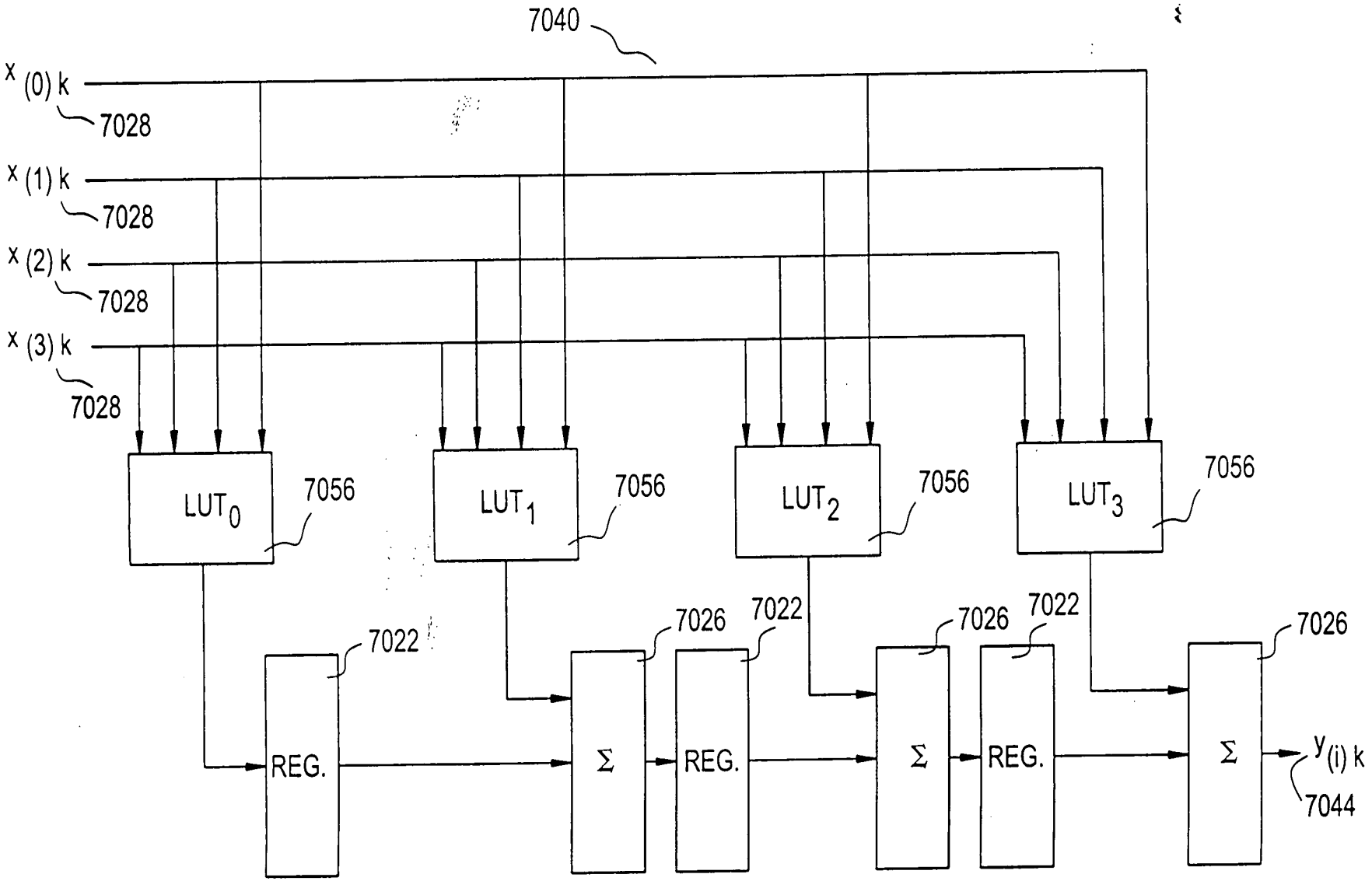

Select Only
On Entry
Enable
Precomputed Values
Stored In Memory Array
Address
Input
To LUT
Memory
x0
x1
x2
x3
4 to 16
Address
Decoder
0000
z=0
0001
z= w0 c0 x0
0010
z= w1 c1 x1
0011
z= w1 c1 x1 + w0 c0 x0
1111
z= w3 c3 x3 + w2 c2 x2
+ w1 c1 x1 + w0 c0 x0
Selected Table Entry
Value Is Output
Memory Data
Output Port
Z k

FIG. 80


7040
x (0) k
7028
x (1) k
7028
x (2) k
7028
x (3) k
7028
LUT0
7056
LUT1
7056
LUT2
7056
LUT3
7056
7022
REG.
7026
Σ
7022
REG.
7026
Σ
7022
REG.
7026
Σ
y (i) k
7044